DATA SHEET

TDA8007B
Double multiprotocol IC card interface

Product specification
Supersedes data of 2002 Nov 15

2003 Feb 18

Philips
Semiconductors

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1 FEATURES

- Control and communication through an 8-bit parallel interface, compatible with multiplexed or non-multiplexed memory access
- Specific ISO UART with parallel access input/output for automatic convention processing, variable baud rate through frequency or division ratio programming, error management at character level for T = 0 and extra guard time register
- FIFO for 1 to 8 characters in reception mode
- Parity error counter in reception mode and in transmission mode with automatic re-transmission
- Dual V_{CC} generation: 5 V ± 5%, 65 mA (max.); 3 V ± 8%, 50 mA (max.) or 1.8 V ± 10%, 30 mA (max.); with controlled rise and fall times
- Dual cards clock generation (up to 10 MHz), with three times synchronous frequency doubling (f_{XTAL}, $^1/_2f_{XTAL}$, $^1/_4f_{XTAL}$ and $^1/_8f_{XTAL}$)
- Cards clock stop (at HIGH or LOW level) or 1.25 MHz (from internal oscillator) for cards Power-down mode
- Automatic activation and deactivation sequence through an independent sequencer
- Supports the asynchronous protocols T = 0 and T = 1 in accordance with:
  - ISO 7816 and EMV 3.1.1 (TDA8007BHL/C2 and TDA8007BHL/C3)
  - ISO 7816 and EMV 2000 (TDA8007BHL/C3)
- Versatile 24-bit time-out counter for Answer To Reset (ATR) and waiting times processing
- Specific Elementary Time Unit (ETU) counter for Block Guard Time (BGT): 22 in T = 1 and 16 in T = 0
- Minimum delay between two characters in reception mode:
  - in Protocol T = 0:
    - 12 ETU (TDA8007BHL/C2)
    - 11.8 ETU (TDA8007BHL/C3)
  - in Protocol T = 1:
    - 11 ETU (TDA8007BHL/C2)
    - 10.8 ETU (TDA8007BHL/C3)
- Supports synchronous cards
- Current limitations in the event of short-circuit (pins I/O1, I/O2, V_{CC1}, V_{CC2}, RST1 and RST2)
- Special circuitry for killing spikes during power-on/power-off
- Supply supervisor for power-on/power-off reset
- Step-up converter (supply voltage from 2.7 to 6 V), doubler, tripler or follower according to V_{CC} and V_{DD}
- Additional input/output pin allowing use of the ISO UART for another analog interface (pin I/OAUX)
- Additional interrupt pin allowing detection of level toggling on an external signal (pin INTAUX)
- Fast and efficient swapping between the three cards due to separate buffering of parameters for each card
- Chip select input allowing use of several devices in parallel and memory space paging
- Enhanced ESD protections on card side: 6 kV (min.)
- Software library for easy integration within the application
- Power-down mode for reducing current consumption when no activity.

2 APPLICATIONS

- Multiple smart card readers for multiprocessor applications (EMV banking, digital pay TV and access control, etc.).

3 GENERAL DESCRIPTION

The TDA8007BHL/C is a cost-effective card interface for dual smart card readers. Controlled through a parallel bus, it meets all requirements of:

ISO 7816, GSM 11-11 and EMV 3.1.1 (TDA8007BHL/C2 and TDA8007BHL/C3)

ISO 7816, GSM 11-11 and EMV 2000 (TDA8007BHL/C3).

It may be interfaced to the ports P0, P1 and P2 of a 80C51 family microcontroller, and be addressed as a memory through MOVX instructions. It may also be addressed on a non-multiplexed 8-bit data bus, by means of address registers AD0, AD1, AD2 and AD3. The integrated ISO UART and the time-out counters allow easy use even at high baud rates with no real time constraints. Due to its chip select, external input/output and interrupt features, it greatly simplifies the realization of a reader of any number of cards. It gives the cards and the reader a very high level of security, due to its special hardware against ESD, short-circuiting, power failure, etc. The integrated step-up converter allows operation within a supply voltage range of 2.7 to 6 V; it may be supplied with a voltage higher than the IC's supply.

A software library has been developed that covers all actions required for T = 0 and T = 1 and synchronous protocols (see application note *"AN01054"*).

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		2.7	–	6	V
V_{DDA}	supply voltage for step-up converter		V_{DD}	–	6	V
$I_{DD(pd)}$	supply current in Power-down mode	V_{DD} = 3.3 V; cards inactive; XTAL oscillator stopped	–	–	350	µA
		V_{DD} = 3.3 V; cards active at V_{CC} = 5 V; CLK stopped; XTAL oscillator stopped	–	–	3	mA
$I_{DD(sm)}$	supply current in sleep mode	cards powered at 5 V; clock stopped	–	–	5.5	mA
$I_{DD(oper)}$	supply current in operating mode	V_{DD} = 3.3 V; f_{XTAL} = 20 MHz; $V_{CC1} = V_{CC2}$ = 5 V; $I_{CC1} + I_{CC2}$ = 80 mA	–	–	315	mA
V_{CC}	card supply output voltage	5 V card				
		including static loads	4.75	5.0	5.25	V
		with 40 nC dynamic loads on 200 nF capacitor	4.6	–	5.4	V
		3 V card				
		including static loads	2.78	–	3.22	V
		with 24 nC dynamic loads on 200 nF capacitor	2.75	–	3.25	V
		1.8 V card				
		including static loads	1.65	–	1.95	V
		with 12 nC dynamic loads on 200 nF capacitor	1.62	–	1.98	V
I_{CC}	card supply output current	5 V card; operating	–	–	65	mA
		3 V card; operating	–	–	50	mA
		1.8 V card; operating	–	–	30	mA
		overload detection	–	100	–	mA
$I_{CC1} + I_{CC2}$	sum of both card supply output currents	operating; 5 and 3 V cards	–	–	80	mA
SR	slew rate on V_{CC} (rise and fall)	$C_{L(max)}$ = 300 nF	0.05	0.16	0.22	V/µs
t_{deact}	deactivation cycle duration		–	–	150	µs
t_{act}	activation cycle duration		–	–	225	µs
f_{XTAL}	crystal frequency		4	–	20	MHz
f_{ext}	external frequency	applied to pin XTAL1	0	–	20	MHz
T_{amb}	ambient temperature		–40	–	+85	°C

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8007BHL/C2	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
TDA8007BHL/C3	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

6 BLOCK DIAGRAM

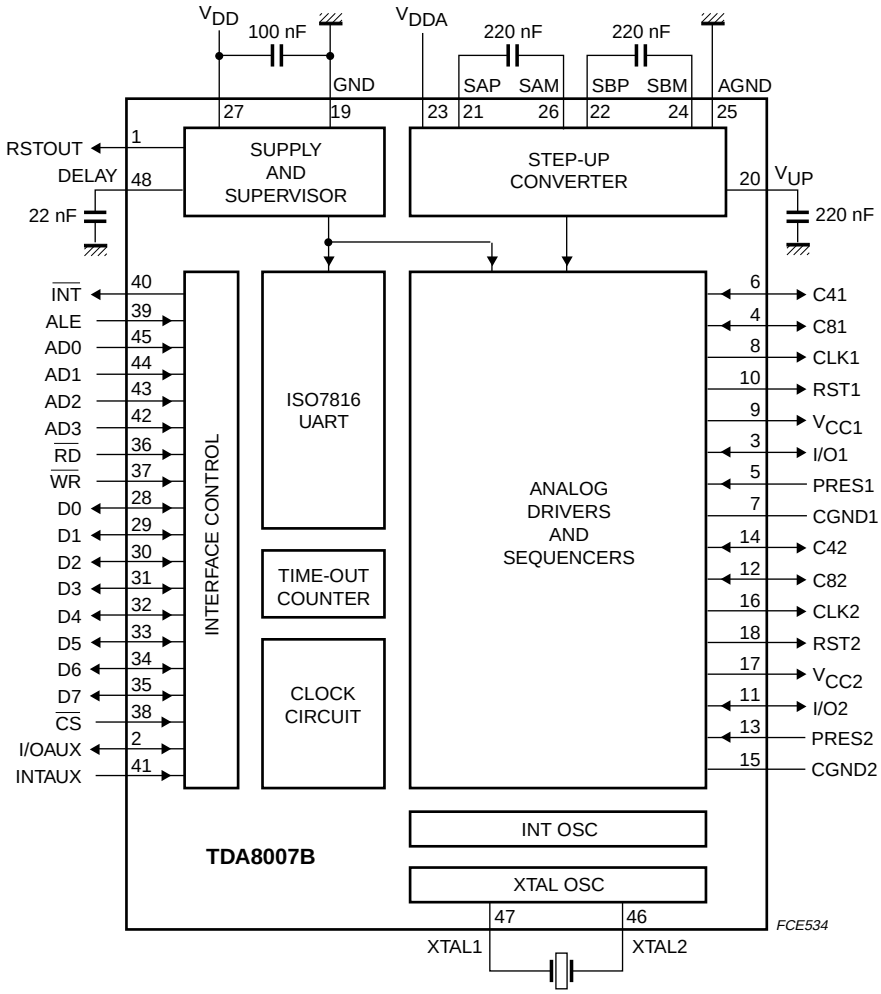


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	DESCRIPTION
RSTOUT	1	PMOS open-drain output for resetting external devices
I/OAUX	2	input or output for an I/O line from an auxiliary smart card interface
I/O1	3	input or output for the data line to/from card 1 (ISO C7 contact)
C81	4	auxiliary I/O for ISO C8 contact (synchronous cards, for instance) for card 1
PRES1	5	card 1 presence contact input (active HIGH)
C41	6	auxiliary I/O for ISO C4 contact (synchronous cards, for instance) for card 1
CGND1	7	ground for card 1; must be connected to GND
CLK1	8	clock output to card 1 (ISO C3 contact)
V_{CC1}	9	card 1 supply output voltage (ISO C1 contact)
RST1	10	card 1 reset output (ISO C2 contact)
I/O2	11	input or output for the data line to/from card 2 (ISO C7 contact)
C82	12	auxiliary I/O for ISO C8 contact (synchronous cards, for instance) for card 2
PRES2	13	card 2 presence contact input (active HIGH)
C42	14	auxiliary I/O for ISO C4 contact (synchronous cards, for instance) for card 2
CGND2	15	ground for card 2; must be connected to GND
CLK2	16	clock output to card 2 (ISO C3 contact)
V_{CC2}	17	card 2 supply output voltage (ISO C1 contact)
RST2	18	card 2 reset output (ISO C2 contact)
GND	19	ground
V_{UP}	20	connection for the step-up converter capacitor; connect a low ESR capacitor of 220 nF to AGND
SAP	21	contact 1 for the step-up converter; connect a low ESR capacitor of 220 nF between pins SAP and SAM
SBP	22	contact 3 for the step-up converter; connect a low ESR capacitor of 220 nF between pins SBP and SBM
V_{DDA}	23	positive analog supply voltage for the step-up converter; may be higher than V_{DD}; decouple with a good quality capacitor to GND
SBM	24	contact 4 for the step-up converter; connect a low ESR capacitor of 220 nF between pins SBP and SBM
AGND	25	analog ground for the step-up converter
SAM	26	contact 2 for the step-up converter; connect a low ESR capacitor of 220 nF between pins SAP and SAM
V_{DD}	27	positive supply voltage; decouple with a good quality capacitor to GND
D0	28	input/output of data 0 or address 0
D1	29	input/output of data 1 or address 1
D2	30	input/output of data 2 or address 2
D3	31	input/output of data 3 or address 3
D4	32	input/output of data 4 or address 4
D5	33	input/output of data 5 or address 5
D6	34	input/output of data 6 or address 6
D7	35	input/output of data 7 or address 7

SYMBOL	PIN	DESCRIPTION
$\overline{RD}$	36	read selection input; read or write in non-multiplexed configuration (active LOW)
$\overline{WR}$	37	write selection input; enable in case of non-multiplexed configuration (active LOW)
$\overline{CS}$	38	chip select input (active LOW)
ALE	39	address latch enable input in case of multiplexed configuration; connect to V_{DD} in non-multiplexed configuration
$\overline{INT}$	40	NMOS interrupt output (active LOW)
INTAUX	41	auxiliary interrupt input
AD3	42	register selection address 3 input
AD2	43	register selection address 2 input
AD1	44	register selection address 1 input
AD0	45	register selection address 0 input
XTAL2	46	connection for an external crystal
XTAL1	47	connection for an external crystal or input for an external clock signal
DELAY	48	connection for an external delay capacitor

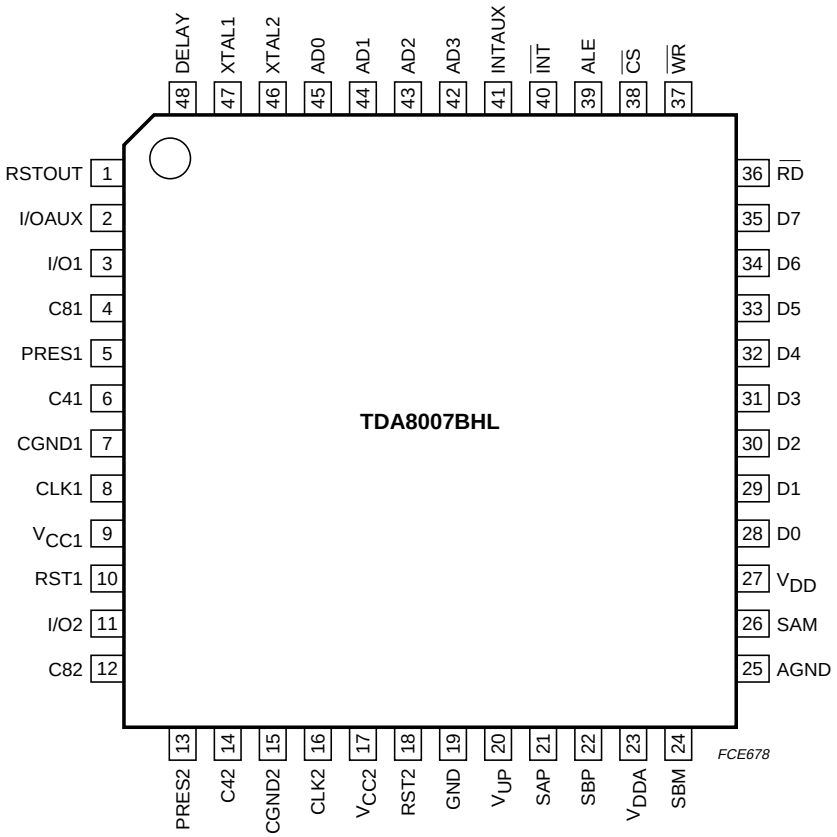


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

Throughout this specification, it is assumed that the reader is aware of *"ISO 7816 norm"* terminology.

8.1 Interface control

The TDA8007BHL/C can be controlled via an 8-bit parallel bus (bits D0 to D7).

8.1.1 MULTIPLEXED CONFIGURATION

If a microcontroller with a multiplexed address and data bus (such as the 80C51) is used, then pins D0 to D7 may be directly connected to ports P0 to P7.

Automatic switching to the multiplexed bus configuration (see Fig.3) occurs:

- In TDA8007BHL/C2; if a rising edge is detected on signal ALE and $\overline{CS}$ is LOW
- In TDA8007BHL/C3; if a rising edge is detected on signal ALE.

In this event, pins AD0 to AD3 play no role and may be tied to V_{DD} or ground.

When signal $\overline{CS}$ = LOW (see Fig.4), the demultiplexing of address and data is performed internally using signal ALE, a LOW pulse on pin $\overline{RD}$ allows the selected register to be read, a LOW pulse on pin $\overline{WR}$ allows the selected register to be written to.

Using a 80C51 microcontroller, the TDA8007BHL/C is simply controlled with MOVX instructions.

8.1.2 NON-MULTIPLEXED CONFIGURATION

If pin ALE is tied to V_{DD} or ground, the TDA8007BHL/C will be in the non-multiplexed configuration. In this case, the address bits are determined by means of pins AD0 to AD3; the read or write control signal is on pin $\overline{RD}$ and a data write or read active LOW enable signal is on pin $\overline{WR}$.

In non-multiplexed bus configuration, signals $\overline{CS}$ and $\overline{WR}$ play the same role.

In read operations (see Fig.5) with signal $\overline{RD}$ = HIGH, the data corresponding to the chosen address is available on the bus when both signals $\overline{CS}$ and $\overline{WR}$ are LOW.

In write operations (see Figs.6 and 7) with signal $\overline{RD}$ = LOW, the data present on the bus is written when signals $\overline{CS}$ and $\overline{WR}$ are LOW.

In both configurations, the TDA8007BHL/C is selected only when signal $\overline{CS}$ = LOW. Signal $\overline{INT}$ is an active LOW interrupt signal.

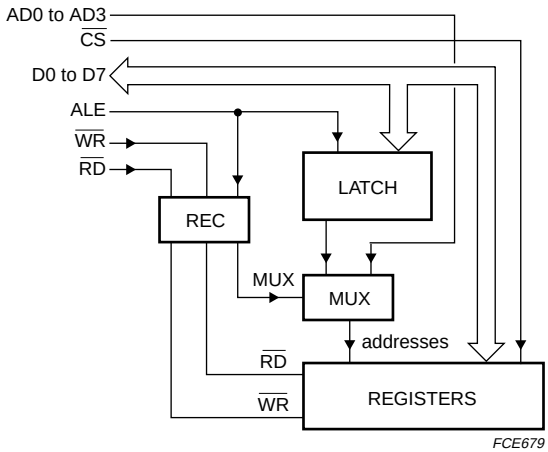


Fig.3 Multiplexed bus recognition.

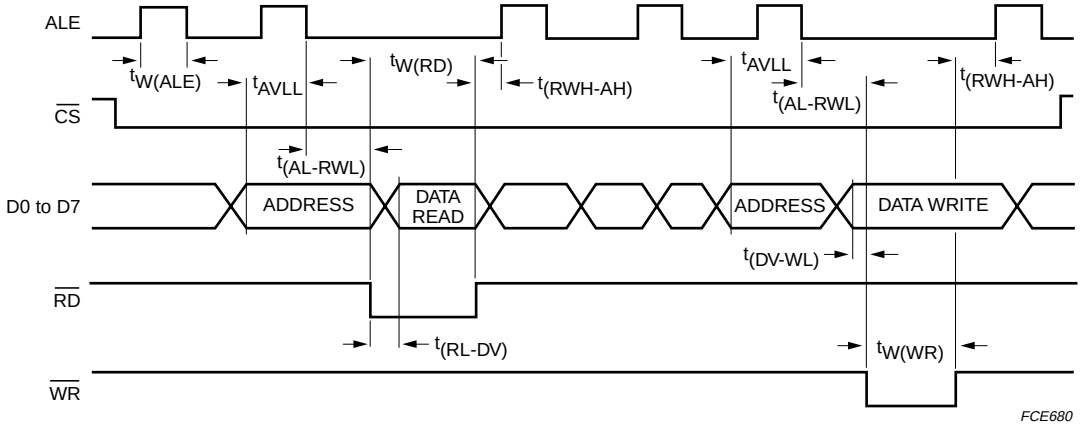


Fig.4 Control with multiplexed bus (read and write).

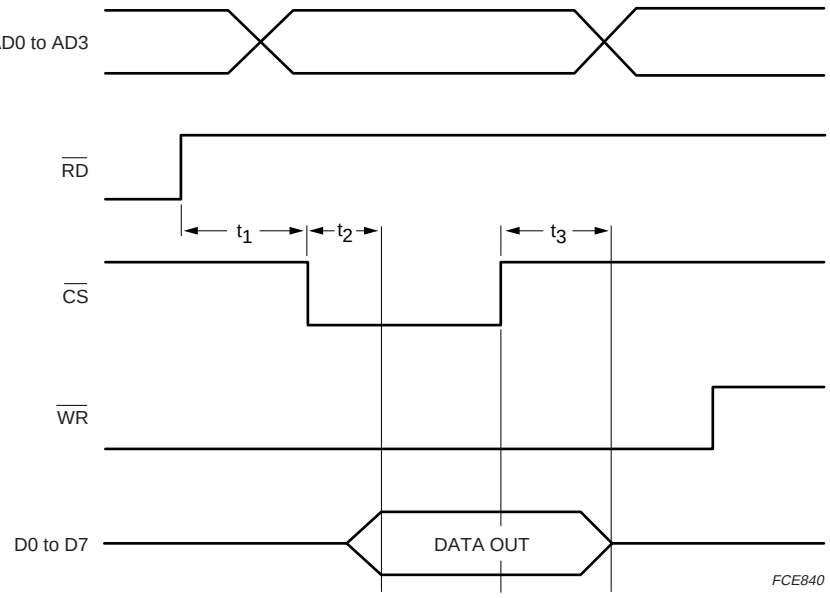


Fig.5 Control with non-multiplexed bus (read).

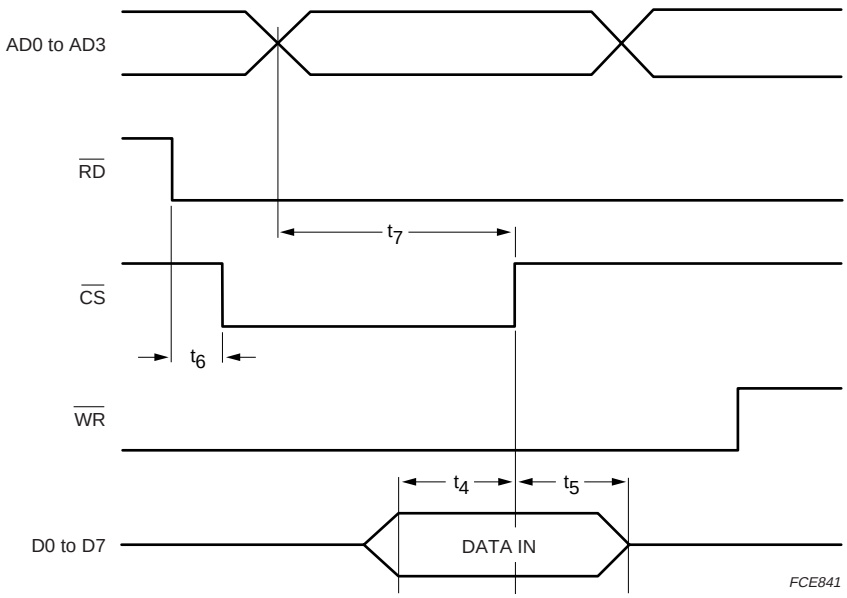


Fig.6 Control with non-multiplexed bus (write release with signal $\overline{CS}$).

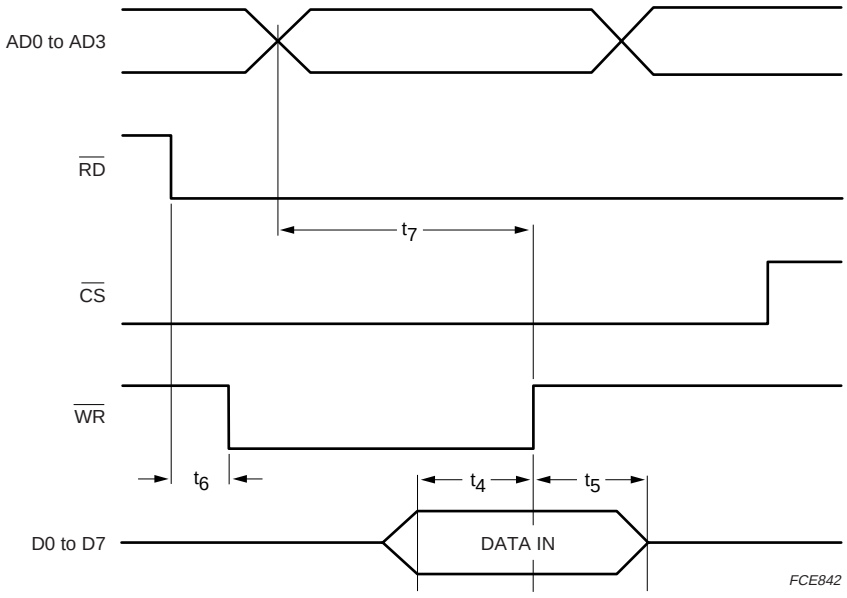


Fig.7 Control with non-multiplexed bus (write release with signal $\overline{EN}$).

8.2 Control registers

The TDA8007BHL/C has two complete analog interfaces which can drive cards 1 and 2. The data to and from these two cards shares the same ISO UART. The data to and from a third card (card 3), externally interfaced (with a TDA8020 or TDA8004 for example), may also share the same ISO UART.

Cards 1, 2 and 3 have dedicated registers for setting the parameters of the ISO UART (see Fig.8):

- Programmable Divider Register (PDR)
- Guard Time Register (GTR)
- UART Configuration Register 1 (UCR1)
- UART Configuration Register 2 (UCR2)
- Clock Configuration Register (CCR).

Cards 1 and 2 also have dedicated registers for controlling their power and clock configuration. The Power Control Register (PCR) for card 3 is controlled externally. Register PCR is also used for writing or reading on the auxiliary card contacts C4 and C8.

Card 1, 2 or 3 can be selected via the Card Select Register (CSR). When one card is selected, the corresponding parameters are used by the ISO UART. Register CSR also contains one bit for resetting the ISO UART (bit $\overline{RIU}$ = 0). This bit is reset after power-on and must be set to logic 1 before starting with any one of the cards. It may be reset by software when necessary.

When the specific parameters of the cards have been programmed, the UART may be used with the following registers:

- UART Receive Register (URR)
- UART Transmit Register (UTR)
- UART Status Register (USR)
- Mixed Status Register (MSR).

In reception mode, a FIFO of 1 to 8 characters may be used and is configured with the FIFO Control Register (FCR). This register is also used for the automatic re-transmission of Not AcKnowledged (NAK) characters in transmission mode.

The Hardware Status Register (HSR) gives the status of the supply voltage, of the hardware protections and of the card movements.

Registers HSR and USR give interrupts on pin $\overline{INT}$ when some of their bits have been changed.

Register MSR does not give interrupts and may be used in the polling mode for some operations; for this use, some of the interrupt sources within the registers USR and HSR may be masked.

A 24-bit time-out counter may be started to give an interrupt after a number of ETU programmed into the Time-Out Registers TOR1, TOR2 and TOR3. This will help the microcontroller in processing different real-time tasks (ATR, WWT, BWT, etc.). This counter is configured with a Time-Out counter Configuration (TOC) register. It may be used as a 24-bit counter or as a 16-bit plus 8-bit counter. Each counter can be set to start counting once data has been written, or on detection of a START bit on the I/O, or as auto-reload.

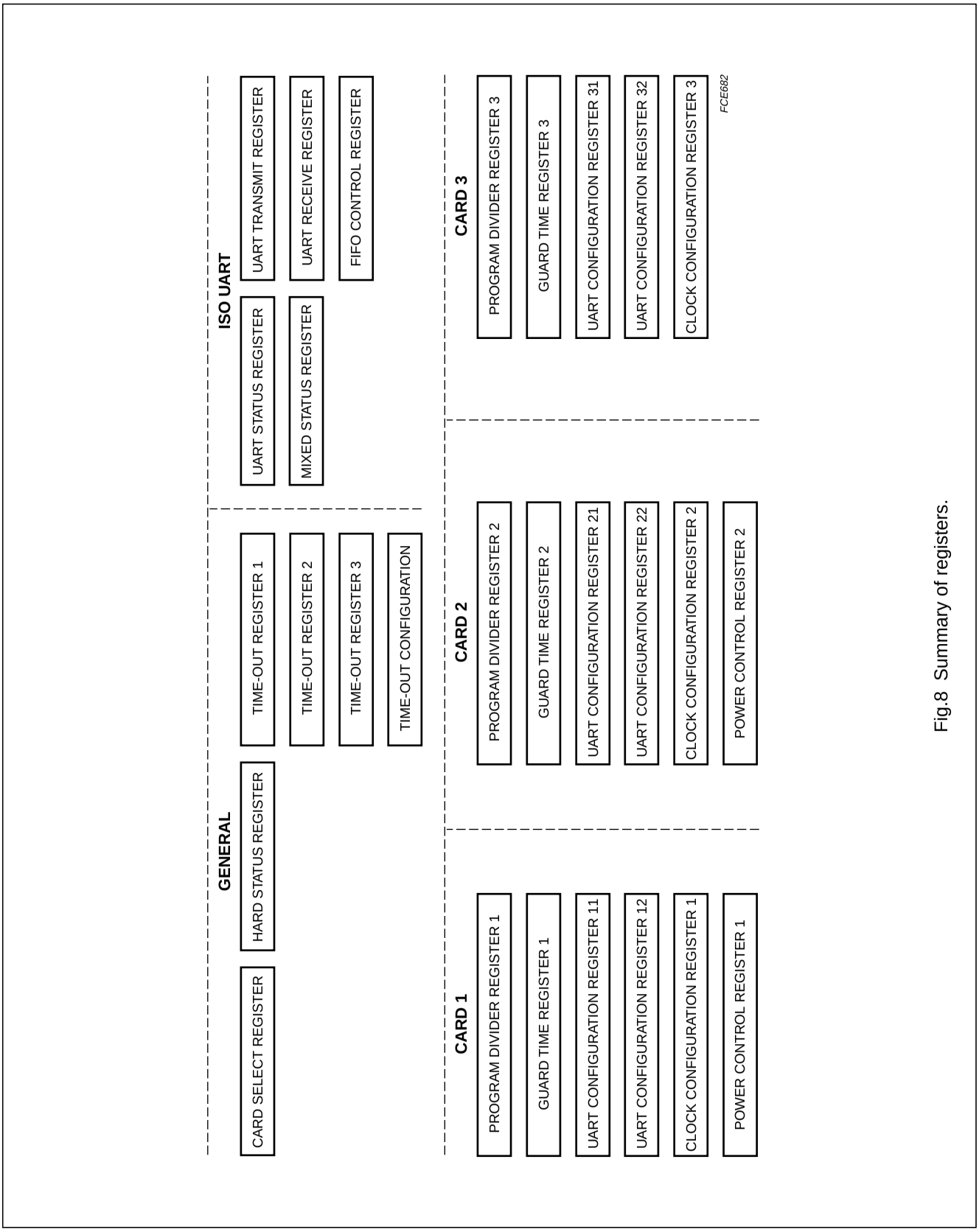


Fig.8 Summary of registers.

8.2.1 GENERAL REGISTERS

8.2.1.1 Card select register

The Card Select Register (CSR) is used for selecting the card on which the UART will act, and also to reset the ISO UART.

Table 1 Register CSR (address 00H; write and read); note 1

7	6	5	4	3	2	1	0
CS7	CS6	CS5	CS4	$\overline{\text{RIU}}$	SC3	SC2	SC1

Note

1. Register value at reset: all significant bits are cleared after reset, except bits CS7 to CS4 which are set to their default value.

Table 2 Description of CSR bits; note 1

BIT	SYMBOL	DESCRIPTION
7	CS7	**IC identification**. Default value for identifying the IC: 0010 = TDA8007BHL/C2 0011 = TDA8007BHL/C3
6	CS6	
5	CS5	
4	CS4	
3	$\overline{\text{RIU}}$	**Reset ISO UART.** When reset, this bit resets a large part of the UART registers to their initial value. Bit $\overline{\text{RIU}}$ must be reset before any activation; logic 0 for at least 10 ns duration. Bit $\overline{\text{RIU}}$ must be set to logic 1 by software before any action on the UART can take place.
2	SC3	**Select Card 3**. If bit SC3 = 1, then card 3 is selected.
1	SC2	**Select Card 2**. If bit SC2 = 1, then card 2 is selected.
0	SC1	**Select Card 1**. If bit SC1 = 1, then card 1 is selected.

Note

1. Bits SC1, SC2 and SC3 must be set one at a time. After reset, no card is selected by default.

8.2.1.2 Hardware status register

The Hardware Status Register (HSR) gives the status of the chip after a hardware problem has been detected.

Table 3 Register HSR (address 0FH; read only); note 1

7	6	5	4	3	2	1	0
HS7	PRTL2	PRTL1	SUPL	PRL2	PRL1	INTAUXL	PTL

Note

1. Register value at reset: all significant bits are cleared after reset, except bit SUPL which is set within pulse RSTOUT.

Table 4 Description of HSR bits.

BIT	SYMBOL	DESCRIPTION
7	HS7	not used
6	PRTL2	**Protection 2**. Bit PRTL2 = 1 when a fault has been detected on card reader 2. Bit PRTL 2 is the OR-function of the protection on pin V_{CC2} and pin RST2.
5	PRTL1	**Protection 1**. Bit PRTL1 = 1 when a fault has been detected on card reader 1. Bit PRTL 1 is the OR-function of the protection on pin V_{CC1} and pin RST1.
4	SUPL	**Supervisor Latch**. Bit SUPL = 1 when the supervisor has been activated.
3	PRL2	**Presence Latch 2**. Bit PRL2 = 1 when a level change has occurred on pin PRES2.
2	PRL1	**Presence Latch 1**. Bit PRL1 = 1 when a level change has occurred on pin PRES1.
1	INTAUXL	**Auxiliary interrupt change**. Bit INTAUXL = 1 if the level on pin INTAUX has been changed.
0	PTL	**Overheating**. Bit PTL = 1 if overheating has occurred.

When at least one of the bits PRTL2, PRTL1, PRL2, PRL1 or PTL is HIGH, then $\overline{INT}$ is LOW. The bits having caused the interrupt are cleared when register HSR has been read-out. The same occurs with INTAUXL, if not disabled.

In case of an emergency deactivation (by bits PRTL2, PRTL1, SUPL, PRL2, PRL1 or PTL), bit START (bit 0 in the PCR) is automatically reset by hardware.

At power-on, or after a supply voltage drop-out, bit SUPL is set and pin $\overline{INT}$ = LOW. Pin $\overline{INT}$ will return to HIGH level at the end of the alarm pulse RSTOUT (see Fig.13).
Bit SUPL will be reset only after a status register read-out outside the alarm pulse.

A minimum time of 2 µs is needed between two successive read operations of register HSR, as well as between reading of register HSR and activation (write in register PCR).

8.2.1.3 Time-out registers

The three Time-Out Registers (TOR1, TOR2 and TOR3) form a programmable 24-bit ETU counter, or two independant counters (one 16-bit and one 8-bit). The value to load in registers TOR1, TOR2 and TOR3 is the number of ETU to count. The time-out counters may only be used when a card is active with a running clock.

Table 5 Register TOR1 (address 09H; write only); note 1

7	6	5	4	3	2	1	0
TOL7	TOL6	TOL5	TOL4	TOL3	TOL2	TOL1	TOL0

Note

1. Register value at reset: all bits are cleared after reset.

Table 6 Register TOR2 (address 0AH; write only); note 1

7	6	5	4	3	2	1	0
TOL15	TOL14	TOL13	TOL12	TOL11	TOL10	TOL9	TOL8

Note

1. Register value at reset: all bits are cleared after reset.

Table 7 Register TOR3 (address 0BH; write only); note 1

7	6	5	4	3	2	1	0
TOL23	TOL22	TOL21	TOL20	TOL19	TOL18	TOL17	TOL16

Note

1. Register value at reset: all bits are cleared after reset.

8.2.1.4 Time-out configuration register

The Time-Out Configuration (TOC) register is used for setting different configurations of the time-out counter as given in Table 9; all other configurations are undefined.

Table 8 Register TOC (address 08H; read and write); note 1

7	6	5	4	3	2	1	0
TOC7	TOC6	TOC5	TOC4	TOC3	TOC2	TOC1	TOC0

Note

1. Register value at reset: all bits are cleared after reset.

Table 9 CARD REGISTERS

TOC VALUE	OPERATING MODE
00H	All counters are stopped.
05H	Counters 2 and 3 are stopped; counter 1 continues to operate in auto-reload mode.
61H	Counter 1 is stopped, and counters 3 and 2 form a 16-bit counter. Counting the value stored in registers TOR3 and TOR2 is started after 61H is written in register TOC. An interrupt is given, and bit TO3 is set within register USR when the terminal count is reached. The counter is stopped by writing 00H in register TOC, and should be stopped before reloading new values in registers TOR2 and TOR3.
65H	Counter 1 is an 8-bit auto-reload counter, and counters 3 and 2 form a 16-bit counter. Counter 1 starts counting the content of register TOR1 on the first START bit (reception or transmission) detected on pin I/O after 65H is written in register TOC. When counter 1 reaches its terminal count, an interrupt is given, bit TO1 in register USR is set, and the counter automatically restarts the same count until it is stopped. It is not allowed to change the content of register TOR1 during a count. Counters 3 and 2 are wired as a single 16-bit counter and start counting the value in registers TOR3 and TOR2 when 65H is written in register TOC. When the counter reaches its terminal count, an interrupt is given and bit TO3 is set within register USR. Both counters are stopped when 00H is written in register TOC. Counters 3 and 2 shall be stopped by writing 05H in register TOC before reloading new values in registers TOR2 and TOR3.
68H	Counters 3, 2 and 1 are wired as a single 24-bit counter. Counting the value stored in registers TOR3, TOR2 and TOR1 is started after 68H is written in register TOC. The counter is stopped by writing 00H in register TOC. It is not allowed to change the content of registers TOR3, TOR2 and TOR1 within a count.
71H	Counter 1 is stopped, and counters 3 and 2 form a 16-bit counter. Counting the value stored in registers TOR3 and TOR2 and is started on the first START bit detected on pin I/O (reception or transmission) after the value has been written, and then on each subsequent START bit. It is possible to change the content of registers TOR3 and TOR2 during a count; the current count will not be affected and the new count value will be taken into account at the next START bit. The counter is stopped by writing 00H in register TOC. In this configuration, registers TOR3, TOR2 and TOR1 must not be all zero.
75H	Counter 1 is an 8-bit auto-reload counter, and counters 3 and 2 form a 16-bit counter. Counter 1 starts counting the content of register TOR1 on the first START bit (reception or transmission) detected on pin I/O after 75H is written in register TOC. When counter 1 reaches its terminal count, an interrupt is given, bit TO1 in register USR is set, and the counter automatically restarts the same count until it is stopped. Changing the content of register TOR1 during a count is not allowed. Counting the value stored in registers TOR3 and TOR2 is started on the first START bit detected on pin I/O (reception or transmission) after the value has been written, and then on each subsequent START bit. It is possible to change the content of registers TOR3 and TOR2 during a count; the current count will not be affected and the new count value will be taken into account at the next START bit. The counter is stopped by writing 00H in register TOC. In this configuration, registers TOR3, TOR2 and TOR1 must not be all zero.

TOC VALUE	OPERATING MODE
7CH	Counters 3, 2 and 1 are wired as a single 24-bit counter. Counting the value stored in registers TOR3, TOR2 and TOR1 is started on the first START bit detected on pin I/O (reception or transmission) after the value has been written, and then on each subsequent START bit. It is possible to change the content of registers TOR3, TOR2 and TOR1 during a count; the current count will not be affected and the new count value will be taken into account at the next START bit. The counter is stopped by writing 00H in register TOC. In this configuration, registers TOR3, TOR2 and TOR1 must not be all zero.
85H	Same as value 05H, except that all the counters will be stopped at the end of the 12th ETU following the first received START bit detected after 85H has been written in register TOC.
E5H	Same configuration as value 65H, except that counter 1 will be stopped at the end of the 12th ETU following the first START bit detected after E5H has been written in register TOC.
F1H	Same configuration as value 71H, except that the 16-bit counter will be stopped at the end of the 12th ETU following the first START bit detected after F1H has been written in register TOC.
F5H	Same configuration as value 75H, except the two counters will be stopped at the end of the 12th ETU following the first START bit detected after F5H has been written in register TOC.

The time-out counter is very useful for processing the clock counting during ATR, the Work Waiting Time (WWT) or the waiting times defined in protocol T = 1. It should be noted that the 200 and n_{max} clock counter (n_{max} = 384 for TDA8007BHL/C2; n_{max} = 368 for TDA8007BHL/C3) used during ATR is done by hardware when the start session is set, specific hardware controls the functionality of BGT in T = 1 and T = 0 protocols and a specific register is available for processing the extra guard time.

Writing to register TOC is not allowed as long as the card is not activated with a running clock.

Before restarting the 16-bit counter (counters 3 and 2) by writing 61H, 65H, 71H, 75H, F1H or F5H in the TOC; or the 24-bit counter (counters 3, 2 and 1) by writing 68H in the TOC; it is mandatory to stop them by writing 00H in the TOC.

Detailed examples of how to use these specific timers can be found in application note *“AN01054”*.

8.2.2 ISO UART REGISTERS

8.2.2.1 UART transmit register

Table 10 Register UTR (address 0DH; write only); note 1

7	6	5	4	3	2	1	0
UT7	UT6	UT5	UT4	UT3	UT2	UT1	UT0

Note

1. Register value at reset: all bits are cleared after reset.

When the microcontroller wants to transmit a character to the selected card, it writes the data in direct convention in the UART Transmit Register (UTR). The transmission:

- Starts at the end of writing (on the rising edge of signal $\overline{WR}$) if the previous character has been transmitted and if the extra guard time has expired
- Starts at the end of the extra guard time if this one has not expired
- Does not start if the transmission of the previous character is not completed
- With a synchronous card (bit SAN within register UCR2 is set), only signal D0 is relevant and is copied on pin I/O of the selected card.

8.2.2.2 UART receive register

Table 11 Register URR (address 0DH; read only); note 1

7	6	5	4	3	2	1	0
UR7	UR6	UR5	UR4	UR3	UR2	UR1	UR0

Note

1. Register value at reset: all bits are cleared after reset.

When the microcontroller wants to read data from the card, it reads it from the UART Receive Register (URR) in direct convention:

- With a synchronous card, only D0 is relevant and is a copy of the state of the selected card I/O
- When needed, this register may be tied to a FIFO whose length ‘n’ is programmable between 1 and 8; if $n > 1$, then no interrupt is given until the FIFO is full and the controller may empty the FIFO when required
- With a parity error:
  - In protocol T = 0; the received byte is not stored in the FIFO and the error counter is incremented. The error counter is programmable between 1 and 8. When the programmed number is reached, then the bit PE is set in the status register USR and $\overline{INT0}$ falls LOW. The error counter must be reprogrammed to the desired value after its count has been reached
  - In protocol T = 1; the character is loaded in the FIFO and the bit PE is set whatever the programmed value in the parity error counter
- When the FIFO is full, then the bit RBF in the status register USR is set. This bit is reset when at least one character has been read from URR
- When the FIFO is empty, then the bit FE is set in the status register USR as long as no character has been received.

8.2.2.3 Mixed status register

The Mixed Status Register (MSR) relates the status of pin INTAUX, the cards presence contacts PRES1 and PRES2, the BGT counter, the FIFO empty indication and the transmit or receive ready indicator TBE/RBF. It also gives useful indications when switching the clock to or from $^1/_2 f_{int}$ and when driving the TDA8007BHL/C with fast controllers.

No bits within register MSR act upon signal $\overline{INT}$.

Table 12 Register MSR (address 0CH; read only); note 1

7	6	5	4	3	2	1	0
CLKSW	FE	BGT	CRED	PR2	PR1	INTAUX	TBE/RBF

Note

1. Register value at reset: bits TBE/RBF, BGT and CLKSW are cleared after reset; bits FE and CRED are set after reset.

Table 13 Description of MSR bits.

BIT	SYMBOL	DESCRIPTION
7	CLKSW	**Clock switch**. Bit CLKSW is set when the TDA8007BHL/C has performed a required clock switch from $\frac{1}{n}f_{XTAL}$ to $\frac{1}{2}f_{int}$, and is reset when the TDA8007BHL/C has performed a required clock switch from $\frac{1}{2}f_{int}$ to $\frac{1}{n}f_{XTAL}$. The application must wait until this bit is set or reset before sending a new command to the card. This bit is reset at power-on.
6	FE	**FIFO Empty**. Bit FE is set when the reception FIFO is empty. It is reset when at least one character has been loaded in the FIFO.
5	BGT	**Block Guard Time**. In protocol T = 1, bit BGT is linked with a 22-ETU counter which is started at every START bit on pin I/O. Bit BGT is set if the count is finished before the next START bit. This helps to verify that the card has not answered before 22 ETU after the last transmitted character, or that the reader is not transmitting a character before 22 ETU after the last received character. In protocol T = 0, bit BGT is linked with a 16-ETU counter which is started at every START bit on pin I/O. Bit BGT is set if the count is finished before the next START bit. This helps to verify that the reader is not transmitting a character before 16 ETU after the last received character.
4	CRED	**Control ready**. It is advised bit CRED is used for driving the TDA8007BHL/C with high speed controllers. Before writing in registers TOC or UTR, or reading from register URR, check if bit CRED is set. If reset, it means that the writing or reading operation will not be correct because the controller is acting faster than the required time for this operation: • 3 clock cycles after rising edge $\overline{RD}$ for reading from register URR: $t_{RD(URR)} - t_{W(RD)}$ (see Fig.9). • 3 clock cycles after rising edge $\overline{WR}$ for writing in register UTR: $t_{WR(UTR)} - t_{W(WR)}$ (see Fig.10) • $\frac{3}{31}$ or $\frac{3}{32}$ ETU after rising edge $\overline{WR}$ for writing in register TOC: $t_{WR(TOC)} - t_{W(WR)}$ (see Fig.11) Bit CRED is set at power-on.
3	PR2	**Card 2 present**. Bit PR2 = 1 when card 2 is present.
2	PR1	**Card 1 present**. Bit PR1 = 1 when card 1 is present.
1	INTAUX	**Auxiliary interrupt**. Bit INTAUX is set when pin INTAUX = HIGH and it is reset when pin INTAUX = LOW.
0	TBE/RBF	**Transmit Buffer Empty/Receive Buffer Full**. Bit TBE/RBF = 1 when: • Changing from reception mode to transmission mode • A character has been transmitted by the UART • The reception FIFO is full. Bit TBE/RBF = 0 after power-on or after one of the following: • When bit RIU is reset • When a character has been written to register UTR • When at least one character has been read in the FIFO • When changing from transmission mode to reception mode.

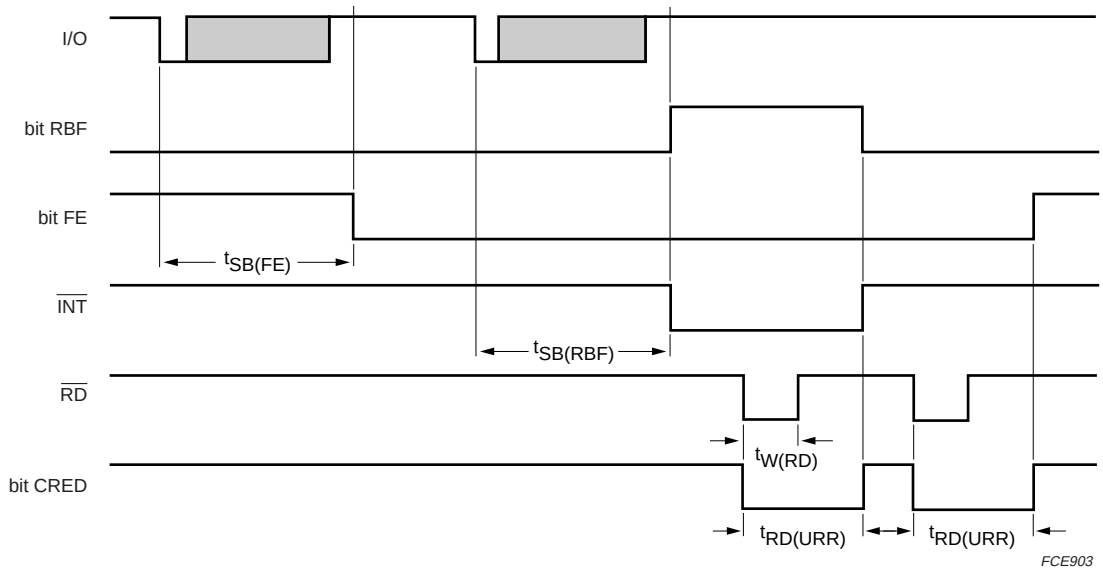


Fig.9 Minimum time between two read operations in register URR.

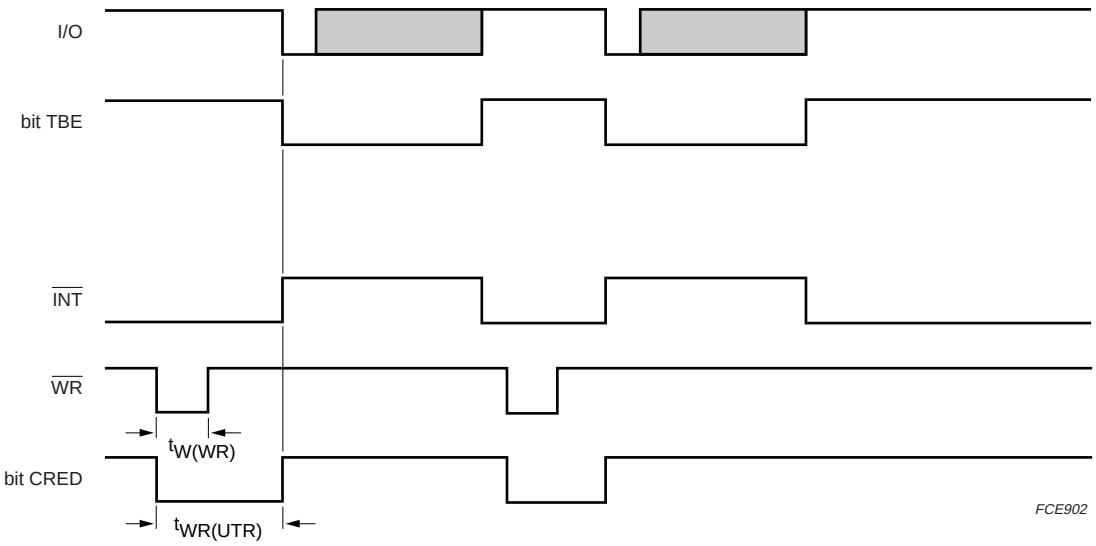


Fig.10 Minimum time between two write operations in register UTR.

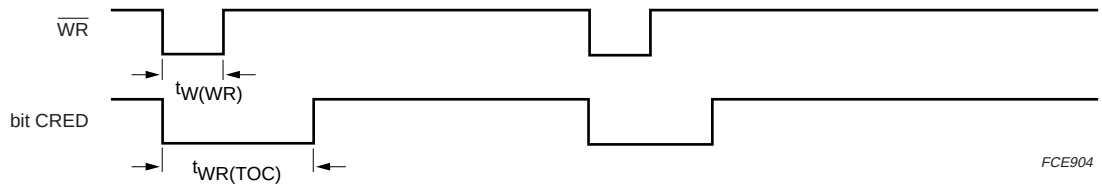


Fig.11 Minimum time between two write operations in register TOC.

8.2.2.4 FIFO control register

The FIFO Control Register (FCR) relates the parity error count and the FIFO length.

Table 14 Register FCR (address 0CH; write only); note 1

7	6	5	4	3	2	1	0
FC7	PEC2	PEC1	PEC0	FC3	FL2	FL1	FL0

Note

1. Register value at reset: all relevant bits are cleared after reset.

Table 15 Description of FCR bits.

BIT	SYMBOL	DESCRIPTION
7	FC7	not used
6	PEC2	**Parity Error Count**. Bits PEC2, PEC1 and PEC0 determine the number of allowed repetitions in reception or in transmission before setting bit PE in register USR and pulling pin $\overline{INT}$ to LOW level. The value 000 indicates that, if only one parity error has occurred, bit PE is set; the value 111 indicates that bit PE will be set after 8 parity errors. In protocol T = 0: • If a correct character is received before the programmed error number is reached, the error counter will be reset • If the programmed number of allowed parity errors is reached, bit PE in register USR will be set as long as register USR has not been read • If a transmitted character has been NAK by the card, then the TDA8007BHL/C will automatically re-transmit it a number of times equal to the value programmed in bits PEC2, PEC1 and PEC0; the character will be resent at 15 ETU • In transmission mode, if bits PEC2, PEC1 and PEC0 are logic 0, then the automatic re-transmission is invalidated; the character manually rewritten in register UTR will start at 13.5 ETU. In protocol T = 1: • The error counter has no action: bit PE is set at the first incorrectly received character.
5	PEC1	
4	PEC0	
3	FC3	not used
2	FL2	**FIFO length**. Bits FL2, FL1 and FL0 determine the depth of the FIFO: • 000 = length 1 • 111 = length 8.
1	FL1	
0	FL0	

8.2.2.5 UART status register

The UART Status Register (USR) is used by the microcontroller to monitor the activity of the ISO UART and that of the time-out counter. If any of the status bits FER, OVR, PE, EA, TO1, TO2 or TO3 are set, then signal $\overline{INT}$ = LOW. The bit having caused the interrupt is reset 2 μs after the rising edge of signal $\overline{RD}$ during a read operation of register USR.

If bit TBE/RBF is set and if the mask bit DISTBE/RBF within register UCR2 is not set, then also signal $\overline{INT}$ = LOW. Bit TBE/RBF is reset 3 clock cycles after data has been written in register UTR, or 3 clock cycles after data has been read from register URR, or when changing from transmission mode to reception mode.

In order to avoid counting these clock cycles, bit CRED (described in register MSR) may be used.

If LCT mode is used for transmitting the last character, then bit TBE is not set at the end of the transmission.

Table 16 Register USR (address 0EH; read only); note 1

7	6	5	4	3	2	1	0
TO3	TO2	TO1	EA	PE	OVR	FER	TBE/RBF

Note

1. Register value at reset: all bits are cleared after reset.

Table 17 Description of USR bits.

BIT	SYMBOL	DESCRIPTION
7	TO3	**Time-Out counter 3**. Bit TO3 is set when counter 3 has reached its terminal count.
6	TO2	**Time-Out counter 2**. Bit TO2 is set when counter 2 has reached its terminal count.
5	TO1	**Time-Out counter 1**. Bit TO1 is set when counter 1 has reached its terminal count.
4	EA	**Early Answer** is HIGH if the first START bit on the I/O during ATR has been detected between the first 200 and n_{max}(1) clock pulses with RST LOW (all activities on the I/O during the first 200 clock pulses with RST LOW are not taken into account) and before the first n_{max}(1) clock pulses with RST HIGH. These two features are re-initialized at each toggling of RST
3	PE	**Parity Error**. In protocol T = 0, bit PE = 1 if the UART has detected a number of received characters with parity errors equal to the number written in bits PEC2, PEC1 and PEC0 or if a transmitted character has been NAK by the card a number of times equal to the value programmed in bits PEC2, PEC1 and PEC0. It is set at 10.5 ETU in the reception mode and at 11.5 ETU in the transmission mode. In protocol T = 0, a character received with a parity error is not stored in register FIFO (the card should repeat this character). In protocol T = 1, a character with a parity error is stored in the FIFO and the parity error counter is not active.
2	OVR	**Overrun**. Bit OVR = 1 if the UART has received a new character whilst register FIFO was full. In this case, at least one character has been lost.
1	FER	**Framing Error**. Bit FER = 1 when pin I/O was not in the high-impedance state at 10.25 ETU after a START bit. It is reset when register USR has been read-out.
0	TBE/RBF	**Transmission Buffer Empty/Reception Buffer Full**. Bits TBE and RBF share the same bit within register USR: when in transmission mode the relevant bit is TBE; when in reception mode it is RBF. Bit TBE = 1 when the UART is in transmission mode and when the microcontroller may write the next character to transmit in register UTR. It is reset when the microcontroller has written data in the transmit register or when bit T/R within register UCR1 has been reset either automatically or by software. After detection of a parity error in transmission, it is necessary to wait 13.5 ETU before rewriting the character which has been NAK by the card. (Manual mode, see Table 15). Bit RBF = 1 when register FIFO is full. The microcontroller may read some of the characters in register URR, which clears bit RBF.

Note

1. n_{max} = 384 for TDA8007BHL/C2; n_{max} = 368 for TDA8007BHL/C3.

8.2.3 CARD REGISTERS

When cards 1, 2 or 3 are selected, the following registers may be used for programming some specific parameters.

8.2.3.1 Programmable divider register

The Programmable Divider Registers (PDR1, PDR2 and PDR3) are used for counting the cards clock cycles forming the ETU (see Fig.12). These are auto-reload 8-bit counters.

Table 18 Registers PDR1, PDR2 and PDR3 (address 02H; read and write); note 1

7	6	5	4	3	2	1	0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Note

1. Register value at reset: all bits are cleared after reset.

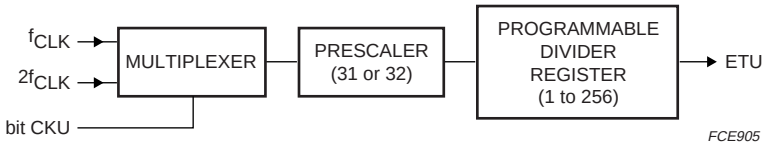


Fig.12 Elementary Time Unit (ETU) generation.

8.2.3.2 UART configuration register 2

The UART Configuration Registers 2 (UCR12, UCR22 and UCR32) relate the UART configuration.

Table 19 Registers UCR12, UCR22 and UCR32 (address 03H; read and write); note 1

7	6	5	4	3	2	1	0
UC27	DISTBE/RBF	DISAUX	PDWN	SAN	$\overline{\text{AUTOCONV}}$	CKU	PSC

Note

1. Register value at reset: all relevant bits are cleared after reset.

Table 20 Description of UCR2 bits.

BIT	SYMBOL	DESCRIPTION
7	UC27	not used
6	DISTBE/RBF	**Disable TBE/RBF interrupt bit**. If bit DISTBE/RBF = 1, then reception or transmission of a character will not generate an interrupt. This feature is useful for increasing communication speed with the card; in this case, a copy of the bit TBE/RBF within register MSR must be polled (and not the original) in order not to lose priority interrupts which can occur in register USR.
5	DISAUX	**Disable auxiliary interrupt**. If bit DISAUX in register UCR2 is set, then a change on pin INTAUX will not generate an interrupt, but bit INTAUXL will be set. Therefore, it is necessary to read register HSR before bit DISAUX is to be reset to avoid an interrupt by bit INTAUXL. In order to avoid an interrupt during a change of card, it is better to set bit DISAUX in register UCR2 for all cards.
4	PDWN	**Power-down mode**. If bit PDWN is set by software, the crystal oscillator is stopped. This mode allows low power consumption in applications where this is required. During the Power-down mode, it is not possible to select a card other than the one currently selected. There are five ways of escaping from the Power-down mode: • Insert card 1 or card 2 • Withdraw card 1 or card 2 • Select the TDA8007BHL/C by resetting bit CS (this assumes that the TDA8007BHL/C had been deselected after setting Power-down mode) • Bit INTAUXL has been set due to a change on pin INTAUX • If pin CS = LOW permanently, reset bit PDWN by software. After any of these events, the TDA8007BHL/C will leave the Power-down mode. Except in the case of a read operation of register HSR, signal $\overline{INT}$ will be pulled to LOW level. The system microcontroller may then read the status registers after 5 ms, and signal $\overline{INT}$ will return to HIGH level (if the system microcontroller has woken the TDA8007BHL/C by re-selecting it, then no bits will be set in the status registers). Note that the Power-down mode can only be entered if bit SUPL has been cleared.
3	SAN	**Synchronous/asynchronous card**. Bit SAN = 1 by software if a synchronous card is expected. The UART is then bypassed and only bit 0 in registers URR and UTR is connected to pin I/O. In this case the clock is controlled by bit SC in register CCR.
2	$\overline{AUTOCONV}$	**Auto convention**. If bit $\overline{AUTOCONV}$ = 1, then the convention is set by software using bit CONV in register UCR1. If the bit is reset, then the configuration is automatically detected on the first received character whilst the start session (bit SS) is set. Bit $\overline{AUTOCONV}$ must not be changed during a card session.
1	CKU	**Clock UART**. For baud rates other than those given in Table 21, there is the possibility to set bit CKU = 1. In this case, the ETU will last half the number of card clock cycles equal to prescaler PDRx. Note that bit CKU = 1 has no effect if $f_{CLK} = f_{XTAL}$. This means, for example, that 76800 baud is not possible when the card is clocked with the external frequency on pin XTAL1.
0	PSC	**PreScale Select**. If bit PSC = 1, then the prescaler value is 32. If bit PSC = 0, then the prescaler value is 31. One ETU will last a number of cards clock cycles equal to prescaler PDRx. All baud rates specified in the ISO 7816 norm are achievable with this configuration (see Table 21).

Table 21 Baud rate selection using values F and D; card clock frequency f_{CLK} = 3.58 MHz for PSC = 31 and f_{CLK} = 4.92 MHz for PSC = 32 (example; in the table 31;12 means prescaler set to 31 and PDR set to 12)

D	F											
	0	**1**	**2**	**3**	**4**	**5**	**6**	**9**	**10**	**11**	**12**	**13**
1	31;12 9600	31;12 9600	31;18 6400	31;24 4800	31;36 3200	31;48 2400	31;60 1920	32;16 9600	32;24 6400	32;32 4800	32;48 3200	32;64 2400
2	31;6 19200	31;6 19200	31;9 12800	31;12 9600	31;18 6400	31;24 4800	31;30 3840	32;8 19200	32;12 12800	32;16 9600	32;24 6400	32;32 4800
3	31;3 38400	31;3 38400		31;6 19200	31;9 12800	31;12 9600	31;15 7680	32;4 38400	32;6 25600	32;8 19200	32;12 12800	32;16 9600
4				31;3 38400		31;6 19200		32;2 76800	32;3 51300	32;4 38400	32;6 25600	32;8 19200
5						31;3 38400		32;1 153600		32;2 76800	32;3 51300	32;4 38400
6										32;1 153600		32;2 76800
8	31;1 115200	31;1 115200		31;2 57600	31;3 38400	31;4 28800	31;5 23040		32;2 76800		32;4 38400	
9							31;3 38400					

8.2.3.3 Guard time register

The Guard Time Registers (GTR1, GTR2 and GTR3) are used for storing the number of guard ETU given by the card during ATR. In transmission mode, the UART will wait this number of ETU before transmitting the character stored in register UTR.

When register GTRx = FF:

- In protocol T = 1
  - TDA8007BHL/C2 operates at 11 ETU
  - TDA8007BHL/C3 operates at 10.8 ETU
- In protocol T = 0
  - TDA8007BHL/C2 operates at 12 ETU
  - TDA8007BHL/C3 operates at 11.8 ETU.

Table 22 Registers GTR1, GTR2 and GTR3 (address 05H; read and write); note 1

7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GT7	GT6	GT5	GT4	GT3	GT2	GT1	GT0

Note

1. Register value at reset: all bits are cleared after reset.

8.2.3.4 UART configuration register 1

The UART Configuration Registers 1 (UCR11, UCR21 and UCR31) set the parameters of the ISO UART.

Table 23 Registers UCR11, UCR21 and UCR31 (address 06H; read and write); note 1

7	6	5	4	3	2	1	0
UC17	FIP	FC	PROT	T/R	LCT	SS	CONV

Note

1. Register value at reset: all relevant bits are cleared after reset.

Table 24 Description of UCR1 bits

BIT	SYMBOL	DESCRIPTION
7	UC17	not used
6	FIP	**Force Inverse Parity**. If bit FIP is set to logic 1, the UART will NAK a correctly received character, and will transmit characters with wrong parity bits.
5	FC	**Test**. Bit FC is a test bit, and must be left at logic 0.
4	PROT	**Protocol**. Bit PROT is set if the protocol is T = 1 (asynchronous) and bit PROT = 0 if the protocol is T = 0.
3	T/R	**Transmit/Receive**. Bit T/R is set by software for transmission mode. A change from logic 0 to 1 will set bit TBE in register USR. Bit T/R is automatically reset by hardware if bit LCT has been used before transmitting the last character.
2	LCT	**Last Character to Transmit**. Bit LCT is set by software before writing the last character to be transmitted in the UTR. It allows automatic change to reception mode. It is reset by hardware at the end of a successful transmission. When LCT is being reset, the bit T/R is also reset and the ISO 7816 UART is ready for receiving a character.
1	SS	**Software convention setting**. Bit SS is set by software before ATR for automatic convention detection and early answer detection. It is automatically reset by hardware at 10.5 ETU after reception of the initial character.
0	CONV	**Convention**. Bit CONV is set if the convention is direct. Bit CONV is either automatically written by hardware according to the convention detected during ATR, or by software if the bit $\overline{\text{AUTOCONV}}$ in register UCR2X is set.

8.2.3.5 Clock configuration registers

The Clock Configuration Registers (CCR1, CCR2 and CCR3) relate the clock signals:

- For cards 1 and 2, register CCRx defines the clock for the selected card
- For cards 1, 2 and 3, register CCRx defines the clock to the ISO UART. It should be noted that, if bit CKU in the prescaler register of the selected card (register UCR2) is set, then the ISO UART is clocked at twice the frequency of the card, which allows baud rates not foreseen in ISO 7816 norm to be reached.

Table 25 Registers CCR1, CCR2 and CCR3 (address 01H; read and write); note 1

7	6	5	4	3	2	1	0
CC7	CC6	SHL	CST	SC	AC2	AC1	AC0

Note

1. Register value at reset: all relevant bits are cleared after reset.

Table 26 Description of CCRx bits

<table>
<tr><th>BIT</th><th>SYMBOL</th><th colspan="4">DESCRIPTION</th></tr>
<tr><td>7</td><td>CC7</td><td colspan="4">not used</td></tr>
<tr><td>6</td><td>CC6</td><td colspan="4">not used</td></tr>
<tr><td>5</td><td>SHL</td><td colspan="4">Stop HIGH or LOW. If bit CST = 1, then the clock is stopped at LOW level if bit SHL = 0, and at HIGH level if bit SHL = 1.</td></tr>
<tr><td>4</td><td>CST</td><td colspan="4">Clock stop. In the case of an asynchronous card, bit CST defines whether the clock to the card is stopped or not; if bit CST is reset, then the clock is determined by bits AC0, AC1 and AC2.</td></tr>
<tr><td>3</td><td>SC</td><td colspan="4">Synchronous clock. In the event of a synchronous card, then contact CLK is the copy of the value of bit SC; in reception mode, the data from the card is available to bit UR0 after a read operation of register URR; in transmission mode, the data is written on the I/O line of the card when register UTR has been written to and remains unchanged when another card is selected.</td></tr>
<tr><td rowspan="9">2 to 0</td><td rowspan="9">AC</td><td colspan="4">Alternating clock. All frequency changes are synchronous, thus ensuring that no spikes or unwanted pulse widths occur during changes.</td></tr>
<tr><td>AC2</td><td>AC1</td><td>AC0</td><td>CLOCK FREQUENCIES (ASYNCHRONOUS CARD)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>f_{XTAL}</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>$\frac{1}{2}f_{XTAL}$</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>$\frac{1}{4}f_{XTAL}$</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>$\frac{1}{8}f_{XTAL}$</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td rowspan="4">$\frac{1}{2}f_{int}$</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>1</td></tr>
</table>

Clock switching constraints:

- f_{int} is the frequency delivered by the internal oscillator
- In case of $f_{CLK} = f_{XTAL}$, the duty cycle must be ensured by the incoming clock signal on pin XTAL1
- When switching from $\frac{1}{n}f_{XTAL}$ to $\frac{1}{2}f_{int}$ or vice verse, only bit AC2 must be changed (bits AC1 and AC0 must remain the same). When switching from $\frac{1}{n}f_{XTAL}$ or $\frac{1}{2}f_{int}$ to clock stopped or vice verse, only bits CST and SHL must be changed
- When switching from $\frac{1}{n}f_{XTAL}$to $\frac{1}{2}f_{int}$ or vice verse, a delay can occur between the command and the effective frequency change on CLK (the fastest switching time is from $\frac{1}{2}f_{XTAL}$ to $\frac{1}{2}f_{int}$ or vice verse, the best for duty cycle is from $\frac{1}{8}f_{XTAL}$ to $\frac{1}{2}f_{int}$ or vice verse)
- It is necessary to survey the bit CLKSW in register MSR before re-transmitting commands to the card.

8.2.3.6 Power control registers

The Power Control Registers (PCR1 and PCR2):

- Start or stop card sessions
- Read from or write to auxiliary card contacts C4 and C8
- Are available only for cards 1 or 2.

To deactivate the card, only bit START should be reset.

Table 27 Registers PCR1 and PCR2 (address 07H; read and write)

7	6	5	4	3	2	1	0
PCR7	PCR6	C8	C4	1V8	RSTIN	3V/5V	START

Note

1. Register value at reset: all relevant bits are cleared after reset.

Table 28 Description of PCRx bits

BIT	SYMBOL	DESCRIPTION
7	PCR7	not used
6	PCR6	not used
5	C8	**Contact 8**. When writing to register PCR, pin C8 will output the value of bit C8. When reading from register PCR, bit C8 will store the value on pin C8.
4	C4	**Contact 4**. When writing to register PCR, pin C4 will output the value of bit C4. When reading from register PCR, bit C4 will store the value on pin C4.
3	1V8	**1.8 V cards**. If bit 1V8 is set, then V_{CC} = 1.8 V: it should be noted that no specification is guaranteed with this V_{CC} voltage when the supply voltage V_{DD} is inferior to 3 V
2	RSTIN	**Reset bit**. When the card is activated, pin RST is the copy of the value written in bit RSTIN.
1	3V/5V	**3 or 5 V cards**. If bit 3V/5V = 1, then V_{CC} = 3 V; if bit 3V/5V = 0, then V_{CC} = 5 V.
0	START	**Start**. If the microcontroller sets bit START = 1, then the selected card is activated (see Section 8.6); if the microcontroller resets bit START = 0, then the card is deactivated (see Section 8.7). Bit START is automatically reset in case of emergency deactivation. To deactivate the card, only bit START should be reset.

8.2.4 REGISTER SUMMARY

Table 29 Register summary

ADDR	NAME	R/W	7	6	5	4	3	2	1	0	VALUE AT RESET(2)	VALUE WHEN $\overline{RIU}$ = 0(2)
00	CSR(1)	R/W	0	0	1	0	$\overline{RIU}$	SC3	SC2	SC1	001v 0000(3)	001v 0000(3)
01	CCR(1)	R/W	not used	not used	SHL	CST	SC	AC2	AC1	AC0	XX00 0000	XXuu uuuu
02	PDR(1)	R/W	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	0000 0000	uuuu uuuu
03	UCR2(1)	R/W	not used	DISTBE/ RBF	DISAUX	PDWN	SAN	$\overline{AUTOC}$	CKU	PSC	X000 0000	uuuu uuuu
05	GTR(1)	R/W	GT7	GT6	GT5	GT4	GT3	GT2	GT1	GT0	0000 0000	uuuu uuuu
06	UCR1(1)	R/W	not used	FIP	FC	PROT	T/R	LCT	SS	CONV	X000 0000	Xuuu 00uu
07	PCR(1)	R/W	not used	not used	C8	C4	1V8	RSTIN	3V/5V	START	XX11 0000	XX11 uuuu
08	TOC	R/W	TOC7	TOC6	TOC5	TOC4	TOC3	TOC2	TOC1	TOC0	0000 0000	0000 0000
09	TOR1	W	TOL7	TOL6	TOL5	TOL4	TOL3	TOL2	TOL1	TOL0	0000 0000	uuuu uuuu
0A	TOR2	W	TOL15	TOL14	TOL13	TOL12	TOL11	TOL10	TOL9	TOL8	0000 0000	uuuu uuuu
0B	TOR3	W	TOL23	TOL22	TOL21	TOL20	TOL19	TOL18	TOL17	TOL16	0000 0000	uuuu uuuu
0C	MSR	R	CLKSW	FE	BGT	CRED	PR2	PR1	INTAUX	TBE/RBF	0101 XXX0	u1u1 uuu0
0C	FCR	W	not used	PEC2	PEC1	PEC0	not used	FL2	FL1	FL0	X000 X000	Xuuu Xuuu
0D	URR	R	UR7	UR6	UR5	UR4	UR3	UR2	UR1	UR0	0000 0000	0000 0000
0D	UTR	W	UT7	UT6	UT5	UT4	UT3	UT2	UT1	UT0	0000 0000	0000 0000
0E	USR	R	TO3	TO2	TO1	EA	PE	OVR	FER	TBE/RBF	0000 0000	0000 0000
0F	HSR	R	not used	PRTL2	PRTL1	SUPL	PRL2	PRL1	INTAUXL	PTL	X001 0000	Xuuu XXXu

Notes

1. Registers PDR, GTR, UCR1, UCR2, CCR and PCR vary according to the card selected.
2. X = undefined; u = no change.
3. TDA8007BHL/C2: v = 0; TDA8007BHL/C3: v = 1.

8.3 Supplies and voltage supervisor

The TDA8007BHL/C operates within a supply voltage range of 2.7 to 6 V. The supply pins are V_{DD}, V_{DDA}, GND and AGND.

Pins V_{DDA} and AGND supply the analog drivers to the cards and have to be decoupled externally because of the large current spikes that the cards and the step-up converter can create. V_{DDA} may be different from V_{DD}.

Pins V_{DD} and GND supply the remainder of the chip. An integrated spike killer ensures that the contacts to the cards remain inactive during power-up and power-down. An internal voltage reference is generated for use within the step-up converter, the voltage supervisor and the V_{CC} generators.

The voltage supervisor generates an alarm pulse when V_{DD} is too low to ensure proper operation. The alarm pulse length is defined by an external capacitor tied to pin DELAY and is typically 1 ms per 2 nF.

The alarm pulse may be used as a reset pulse by the system microcontroller (pin RSTOUT = HIGH). It can also be used to block any spurious noise on card contacts during the microcontrollers reset, or to force an automatic deactivation of the contacts in the event of a supply drop-out (see Sections 8.6 and 8.7).

After power-on, or after a voltage drop, bit SUPL is set within register HSR and remains set until register HSR is read-out outside the alarm pulse. Signal $\overline{INT}$ = LOW for the duration that signal RSTOUT is active.

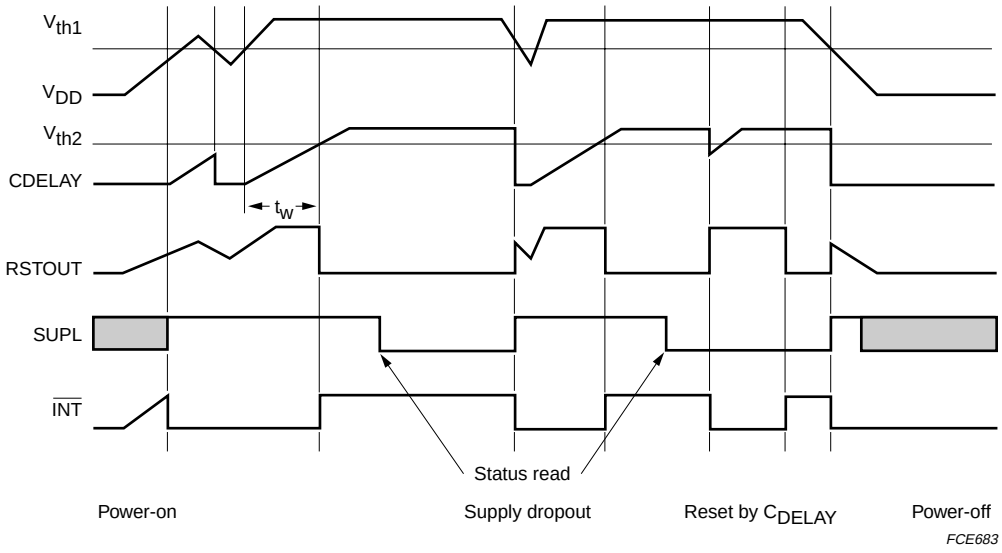


Fig.13 Voltage supervisor.

8.4 Step-up converter

Except for the V_{CC} generator and the other cards contact buffers, the whole circuit is powered by V_{DD} and V_{DDA}. If the supply voltage is 2.5 V, then a higher voltage is needed for the ISO contacts supply. When a card session is requested by the microcontroller, the sequencer first enables the step-up converter (switched capacitors type) which is clocked by an internal oscillator at a frequency of approximately 2.5 MHz.

Supposing that V_{CC} is the maximum of V_{CC1} and V_{CC2}, then the possible situations are:

- V_{CC} = 5 V
  - For V_{DD} = 3 V the step-up converter acts as a voltage tripler with regulation of V_{UP} at approximately 5.5 V
  - For V_{DD} = 5 V the step-up converter acts as a voltage doubler with regulation of V_{UP} at approximately 5.5 V
- V_{CC} = 3 V
  - For V_{DD} = 3 V the step-up converter acts as a voltage doubler with regulation of V_{UP} at approximately 4.0 V
  - For V_{DD} = 5 V the step-up converter acts as a voltage follower and V_{DD} is applied to V_{UP}
- V_{CC} = 1.8 V
  - The step-up converter acts as a voltage follower for any value of V_{DD}.

The recognition of the supply voltage is done by the TDA8007BHL/C at approximately 3.5 V.

The output voltage V_{UP} is fed to the V_{CC} generators. V_{CC} and CGND are used as a reference for all other card contacts.

8.5 ISO 7816 security

The correct sequence during activation and deactivation of the cards is ensured by two specific sequencers, the clock is defined by a division ratio of the internal oscillator.

Activation (bit START = 1 in registers PCR1 or PCR2) is only possible if the card is present (pin PRES is active HIGH with an internal current source to ground) and if the supply voltage is correct (voltage supervisor not active).

The presence of the cards is signalled to the microcontroller by register HSR. Bits PR1 or PR2 in register MSR are set if card 1 or 2 is present. Bits PRL1 or PRL2 are set if pins PRES1 or PRES2 have been toggled.

During a session, the sequencer performs an automatic emergency deactivation on one card in the event of card take-off, or short-circuit. Both cards are automatically deactivated in the event of a supply voltage drop, or overheating. Register HSR is updated and the $\overline{INT}$ line falls so that the system microcontroller is aware of what happened.

8.6 Activation sequence

When the cards are inactive, pins V_{CC}, CLK, RST, C4, C8 and I/O are at LOW level and have a low-impedance with respect to ground. The step-up converter is stopped.

When everything is satisfactory (voltage supply, card present and no hardware problems), the system microcontroller may initiate an activation sequence of a present card.

After selecting the card and leaving the UART reset mode, and then configuring the necessary parameters for the counters and the UART, bit START can be set within register PCR at t_0 (see Fig.14):

1. The step-up converter is started (t_1); if one card was already active, then the step-up converter was already on and nothing more occurs at this step.
2. Pin V_{CC} starts rising (t_2) from 0 to 3 or 5 V with a controlled rise time of 0.17 V/µs (typical).
3. Pin I/O rises to V_{CC} (t_3); pins C4 and C8 also rise if bits C4 and C8 within register PCR have been set to logic 1 (integrated 14 kΩ pull-up resistors to V_{CC}).
4. Clock pulse CLK is sent to the card (t_4) and pin RST is enabled.
5. After a number of CLK pulses that can be counted with the time-out counter, bit RSTIN may be set by software and pin RST will then rise to V_{CC}.
6. The sequencer is clocked by $\frac{1}{64}f_{int}$ which leads to a time interval of t = 25 µs (typical).

Thus:

t_1 = 0 to $\frac{1}{64}t$

$t_2 = t_1 + \frac{3}{2}t$

$t_3 = t_1 + \frac{7}{2}t$

$t_4 = t_1 + 4t$.

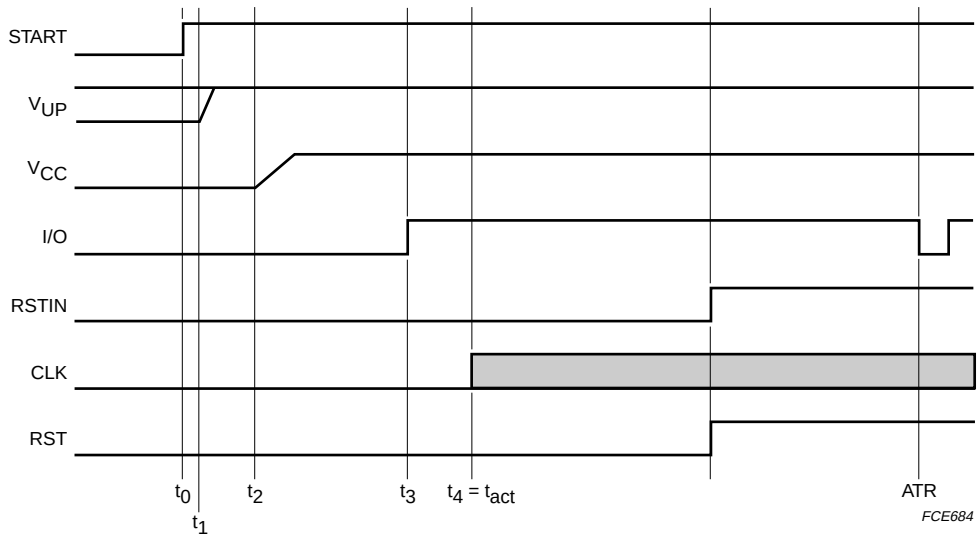


Fig.14 Activation sequence.

8.7 Deactivation sequence

When the session is completed, the microcontroller resets bit START at t_{10}. The circuit then executes an automatic deactivation sequence (see Fig.15):

1. The card is reset by signal RST = LOW (t_{11}).
2. Clock pulse CLK is stopped (t_{12}).
3. Pins I/O, C4 and C8 fall to 0 V (t_{13}).
4. Pin V_{CC} falls to 0 V with typical 0.17 V/µs slew rate (t_{14}).
5. The step-up converter is stopped (t_{15}) and pins CLK, RST, V_{CC} and I/O become low-impedance to ground, if both cards are inactive.

Thus:

$t_{11} = t_{10} + 1/64t$

$t_{12} = t_{11} + 1/2t$

$t_{13} = t_{11} + t$

$t_{14} = t_{11} + 3/2t$

$t_{15} = t_{11} + 7/2t$

t_{de} = time that V_{CC} needs to decrease to less than 0.4 V.

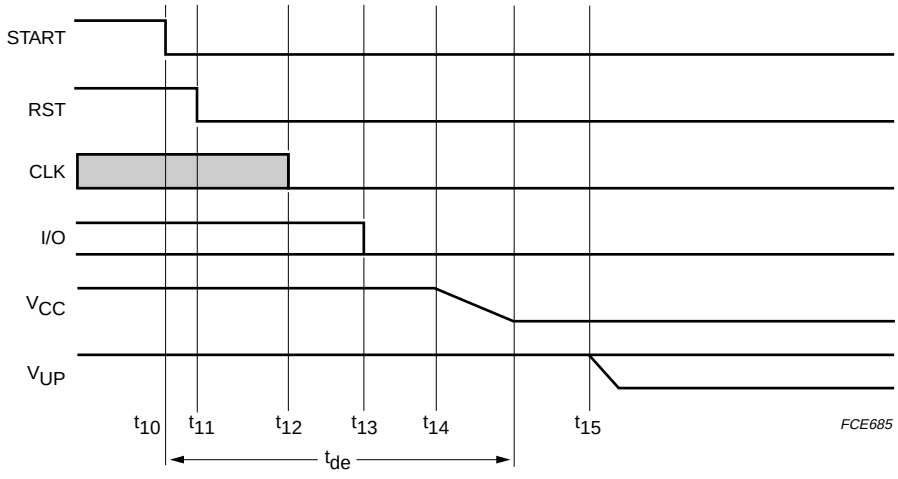


Fig.15 Deactivation sequence.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–0.5	+6.5	V
V_{DDA}	analog supply voltage		–0.5	+6.5	V
V_n	input voltage				
	on pins SAM, SAP, SBM, SBP and V_{UP}		–0.5	+7.5	V
	on all other pins		–0.5	V_{DD} + 0.5	V
P_{tot}	total power dissipation	T_{amb} = –25 to +85 °C	–	700	mW
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–	125	°C
V_{es}	electrostatic discharge voltage	human body model; note 1			
	on pins I/O1, I/O2, V_{CC1}, V_{CC2}, RST1, RST2, CLK1, CLK2, CGND1, CGND2, PRES1 and PRES2		–6	+6	kV
	on pins C41, C42, C81 and C82		–5	+5	kV
	on all other pins		–2	+2	kV

Note

1. Human body model as defined in JEDEC Standard JESD22-A114-B, dated June 2000.

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

11 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	78	K/W

12 CHARACTERISTICS

V_{DD} = 3.3 V; V_{DDA} = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		2.7	–	6.0	V
V_{DDA}	supply voltage for step-up converter		V_{DD}	–	6.0	V
$I_{DD(pd)}$	supply current in Power-down mode	cards inactive; f_{XTAL} = 0 Hz	–	–	350	µA
		cards active; V_{CC} = 5 V; f_{CLK} = 0 Hz; f_{XTAL} = 0 Hz	–	–	3	mA
$I_{DD(sm)}$	supply current in sleep mode	cards active; f_{CLK} = 0 Hz	–	–	5.5	mA
$I_{DD(oper)}$	supply current in operating modem	5 V cards I_{CC1} = 65 mA; I_{CC2} = 15 mA; f_{XTAL} = 20 MHz; f_{CLK} = 10 MHz; V_{DD} = 2.7 V	–	–	315	mA
		3 V cards I_{CC1} = 50 mA; I_{CC2} = 30 mA; f_{XTAL} = 20 MHz; f_{CLK} = 10 MHz				
		V_{DD} = 2.7 V	–	–	215	mA
		V_{DD} = 5 V	–	–	100	mA
Voltage supervisor; see Fig.13						
V_{th1}	threshold voltage on pin V_{DD}	falling	2.10	–	2.50	V
V_{hys1}	hysteresis on V_{th1}		50	–	170	mV
CAPACITOR CONNECTION: PIN DELAY						
V_{th2}	threshold voltage		–	1.25	–	V
V_o	output voltage		–	–	V_{DD} + 0.3	V
I_o	output current	V_{DELAY} = 0 V (charge)	–	–2	–	µA
		V_{DELAY} = V_{DD} (discharge)	–	2	–	mA
C_o	output capacitance		1	–	–	nF
t_W	alarm pulse width	C_{DELAY} = 22 nF	–	10	–	ms
OUTPUT: PIN RSTOUT (open-drain output)						
Active HIGH option						
V_{OH}	HIGH-level output voltage	I_{OH} = –1 mA	0.8V_{DD}	–	V_{DD} + 0.3	V
I_{OL}	LOW-level output current	V_{OL} = 0 V	–	–	–10	µA
Active LOW option						
I_{OH}	HIGH-level output current	V_{OH} = 5 V	–	–	10	µA
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	–0.3	–	+0.4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal oscillator						
f_{XTAL}	crystal frequency		4	–	20	MHz
f_{ext}	external frequency on pin XTAL1		0	–	20	MHz
Step-up converter						
f_{int}	internal oscillator frequency		2	2.5	3.7	MHz
V_{VUP}	voltage on pin V_{UP}	at least one 5 V card	–	5.7	–	V
		both 3 V cards	–	4.1	–	V
$V_{det(dt)}$	detection voltage on pin V_{DD} for doubler or tripler selection		3.4	3.5	3.6	V
Reset output to the cards: pins RST1 and RST2						
$V_{o(inactive)}$	output voltage in inactive mode	no load	0	–	0.1	V
		$I_{o(inactive)}$ = 1 mA	0	–	0.3	V
$I_{o(inactive)}$	output current in inactive mode	V_o = 0 V	0	–	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 200 µA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = –200 µA	V_{CC} – 0.5	–	V_{CC}	V
t_r	rise time	C_L = 30 pF	–	–	0.1	µs
t_f	fall time	C_L = 30 pF	–	–	0.1	µs
Clock output to the cards: pins CLK1 and CLK2						
$V_{o(inactive)}$	output voltage in inactive mode	no load	0	–	0.1	V
		$I_{o(inactive)}$ = 1 mA	0	–	0.3	V
$I_{o(inactive)}$	output current in inactive mode	V_o = 0 V	0	–	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 200 µA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = –200 µA	V_{CC} – 0.5	–	V_{CC}	V
t_r	rise time	C_L = 30 pF	–	–	8	ns
t_f	fall time	C_L = 30 pF	–	–	8	ns
f_{CLK}	clock frequency	idle configuration (1 MHz)	1	–	1.85	MHz
		operational	0	–	10	MHz
δ	duty factor	C_L = 30 pF	45	–	55	%
SR	slew rate (rise and fall)	C_L = 30 pF	0.2	–	–	V/ns
Card supply output voltage: pins V_{CC1} and V_{CC2}; note 1						
$V_{o(inactive)}$	output voltage in inactive mode	no load	0	–	0.1	V
		$I_{o(inactive)}$ = 1 mA	0	–	0.3	V
$I_{o(inactive)}$	output current in inactive mode	V_o = 0 V	–	–	–1	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	output voltage in active mode	5 V card; I_{CC} < 65 mA	4.75	5	5.25	V
		3 V card; I_{CC} < 50 mA	2.78	3	3.22	V
		1.8 V card; I_{CC} < 30 mA	1.65	1.8	1.95	V
		5 V card; current pulses of 40 nC with I < 200 mA, t < 400 ns and f < 20 MHz	4.6	–	5.4	V
		3 V card; current pulses of 24 nC with I < 200 mA, t < 400 ns and f < 20 MHz	2.75	–	3.25	V
		1.8 V card; current pulses of 12 nC with I < 200 mA, t < 400 ns and f < 20 MHz	1.62	–	1.98	V
I_{CC}	output current	5 V card; V_{CC} = 0 to 5 V	–	–	–65	mA
		3 V card; V_{CC} = 0 to 3 V	–	–	–50	mA
		1.8 V card; V_{CC} = 0 to 1.8 V	–	–	–30	mA
$I_{CC1} + I_{CC2}$	sum of both output currents		–	–	–80	mA
SR	slew rate	up or down; maximum capacitance of 300 nF	0.05	0.16	0.22	V/µs
Data lines: pins I/O1 and I/O2; note 2						
R_{pu}	internal pull-up resistance	between pin I/O and V_{CC}	11	14	17	kΩ
$V_{o(inactive)}$	output voltage in inactive mode	no load	0	–	0.1	V
		$I_{o(inactive)}$ = 1 mA	–	–	0.3	V
$I_{o(inactive)}$	output current in inactive mode	V_o = 0 V	–	–	–1	mA
Configured as output						
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} < –20 µA	$0.8V_{CC}$	–	V_{CC} + 0.25	V
		I_{OH} < –40 µA for 5 and 3 V cards	$0.75V_{CC}$	–	V_{CC} + 0.25	V
$t_{o(r)}$, $t_{o(f)}$	output transition time (rise and fall time)	$C_L \leq 30$ pF	–	–	0.1	µs
Configured as input						
V_{IL}	LOW-level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH-level input voltage		1.5	–	V_{CC}	V
I_{IL}	LOW-level input current	V_{IL} = 0 V	–	–	600	µA
I_{LIH}	HIGH-level input leakage current	$V_{IH} = V_{CC}$	–	–	20	µA
$t_{i(r)}$, $t_{i(f)}$	input transition time (rise and fall time)	$C_L \leq 30$ pF	–	–	1.2	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Auxiliary cards contacts: pins C41, C81, C42 and C82; note 3						
$V_{o(inactive)}$	output voltage in inactive mode	no load	0	–	0.1	V
		$I_{o(inactive)}$ = 1 mA	–	–	0.3	V
$I_{o(inactive)}$	output current in inactive mode	V_o = 0 V	–	–	–1	mA
$t_{W(pu)}$	active pull-up pulse width		–	200	–	ns
$R_{int(pu)}$	internal pull-up resistance	between pins C4 or C8 and V_{CC}	8	10	12	kΩ
f_{max}	maximum frequency	on card contact pins	–	–	1	MHz
Configured as output						
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} < –20 μA	$0.8V_{CC}$	–	V_{CC} + 0.25	V
		I_{OH} < –40 μA for 5 and 3 V cards	$0.75V_{CC}$	–	V_{CC} + 0.25	V
$t_{o(r)}$, $t_{o(f)}$	output transition time (rise and fall time)	C_L = 30 pF	–	–	0.1	μs
Configured as input						
V_{IL}	LOW-level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH-level input voltage		1.5	–	V_{CC}	V
I_{IL}	LOW-level input current	V_{IL} = 0 V	–	–	600	μA
I_{LIH}	HIGH-level input leakage current	V_{IH} = V_{CC}	–	–	20	μA
$t_{i(r)}$, $t_{i(f)}$	input transition time (rise and fall time)	C_L = 30 pF	–	–	1.2	μs
Timing						
t_{act}	activation sequence duration	see Fig.14	–	–	130	μs
t_{de}	deactivation sequence duration	see Fig.15	–	–	150	μs
Protection and limitation						
$I_{CC(sd)}$	shutdown and limitation current at pin V_{CC}		–	–100	–	mA
$I_{I/O(lim)}$	limitation current on pin I/O		–15	–	+15	mA
$I_{CLK(lim)}$	limitation current on pin CLK		–70	–	+70	mA
$I_{RST(sd)}$	shutdown current on pin RST		–	–20	–	mA
$I_{RST(lim)}$	limitation current on pin RST		–20	–	+20	mA
T_{sd}	shutdown temperature		–	150	–	°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Card presence inputs: pins PRES1 and PRES2						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	–	V
I_{LIL}	LOW-level input leakage current	V_{IL} = 0 V	–	–	40	µA
I_{LIH}	HIGH-level input leakage current	$V_{IH} = V_{DD}$	–	–	40	µA
Bidirectional data bus: pins D0 to D7						
Configured as input						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	–	V
I_{LIL}	LOW-level input leakage current		–20	–	+20	µA
I_{LIH}	HIGH-level input leakage current		–20	–	+20	µA
C_L	load capacitance		–	–	10	pF
Configured as output						
V_{OL}	LOW-level output voltage	I_{OL} = 5 mA	–	–	$0.2V_{DD}$	V
V_{OH}	HIGH-level output voltage	I_{OH} = –5 mA	$0.8V_{DD}$	–	–	V
$t_{o(r)}$, $t_{o(f)}$	output transition time (rise and fall time)	C_L = 50 pF	–	–	25	ns
Logic inputs: pins ALE, AD0, AD1, AD2, AD3, INTAUX, $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$						
V_{IL}	LOW-level input voltage		–0.3	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
I_{LIL}	LOW-level input leakage current		–20	–	+20	µA
I_{LIH}	HIGH-level input leakage current		–20	–	+20	µA
C_L	load capacitance		–	–	10	pF
Auxiliary input and output: pin I/OAUX; note 4						
$R_{int(pu)}$	internal pull-up resistance	between pin I/OAUX and V_{DD}	11	14	17	kΩ
f_{max}	maximum frequency	on pin I/OAUX	–	–	1	MHz
Configured as input						
V_{IL}	LOW-level input voltage		–0.3	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
I_{LIH}	HIGH-level input leakage current		–20	–	+20	µA
I_{IL}	LOW-level input current	V_{IL} = 0 V	–	–	–600	µA
$t_{i(r)}$, $t_{i(f)}$	input transition time (rise and fall time)	C_L = 30 pF	–	–	1.2	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Configured as output						
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	–	–	300	mV
V_{OH}	HIGH-level output voltage	I_{OH} = 40 μA	$0.75V_{DD}$	–	V_{DD} + 0.25	V
$t_{o(r)}$, $t_{o(f)}$	output transition time (rise and fall time)	C_L = 30 pF	–	–	0.1	μs
Interrupt line: pin $\overline{INT}$ (open-drain output)						
V_{OH}	LOW-level output voltage	I_{OH} = 2 mA	–	–	0.3	V
I_{LIH}	HIGH-level input leakage current		–	–	10	μA

Notes

1. To meet these specifications, two ceramic multilayer capacitors with low ESR of minimum 100 nF should be used.
2. Pin I/O1 has an integrated 14 kΩ pull-up resistance to V_{CC1} and pin I/O2 has an integrated 14 kΩ pull-up resistance to V_{CC2}.
3. Pins C41 and C81 have an integrated 10 kΩ pull-up resistance to V_{CC1} and pins C42 and C82 have an integrated 10 kΩ pull-up resistance to V_{CC2}.
4. Pin I/OAUX has a 14 kΩ pull-up resistance to V_{DD}.

13 TIMING

V_{DD} = 3.3 V; V_{DDA} = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing for multiplexed bus; see Fig.4						
$T_{cy(XTAL1)}$	XTAL1 cycle time		50	–	–	ns
$t_{W(ALE)}$	ALE pulse width		20	–	–	ns
t_{AVLL}	address valid to ALE LOW		10	–	–	ns
$t_{(AL-RWL)}$	ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW		10	–	–	ns
$t_{W(RD)}$	$\overline{RD}$ pulse width	for register URR	$2T_{cy(XTAL1)}$	–	–	ns
		for other registers	10	–	–	ns
$t_{(RL-DV)}$	$\overline{RD}$ LOW to data read valid		–	–	50	ns
$t_{(RWH-AH)}$	$\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH		10	–	–	ns
$t_{W(WR)}$	$\overline{WR}$ pulse width		10	–	–	ns
$t_{(DV-WL)}$	data write valid to $\overline{WR}$ LOW		10	–	–	ns
Timing for non-multiplexed bus						
READ CONTROL; see Fig.5						
t_1	$\overline{RD}$ HIGH to $\overline{CS}$ LOW		10	–	–	ns
t_2	access time $\overline{CS}$ LOW to data out valid		–	–	50	ns
t_3	$\overline{CS}$ HIGH to data out high-impedance		–	–	10	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
WRITE CONTROL; see Figs 6 and 7						
t_4	data valid to end-of-write		10	–	–	ns
t_5	data hold time		10	–	–	ns
t_6	$\overline{RD}$ LOW to $\overline{CS}$ or $\overline{WR}$ LOW		10	–	–	ns
t_7	address stable to $\overline{CS}$ or $\overline{WR}$ HIGH		10	–	–	ns
Timing for bit CRED						
READ OPERATIONS IN UART RECEIVE REGISTER; see Fig.9						
$t_{W(RD)}$	$\overline{RD}$ pulse width		10	–	–	ns
$t_{RD(URR)}$	$\overline{RD}$ LOW to bit CRED = 1		$t_{W(RD)} + 2T_{cy(CLK)}$	–	$t_{W(RD)} + 3T_{cy(CLK)}$	ns
$t_{SB(FE)}$	set time bit FE		10.5	–	–	ETU
$t_{SB(RBF)}$	set time bit RBF		10.5	–	–	ETU
WRITE OPERATIONS IN UART TRANSMIT REGISTER; see Fig.10						
$t_{W(WR)}$	$\overline{WR}$ pulse width		10	–	–	ns
$t_{WR(UTR)}$	$\overline{WR}$ LOW to I/O LOW		$t_{W(WR)} + 2T_{cy(CLK)}$	–	$t_{W(WR)} + 3T_{cy(CLK)}$	ns
WRITE OPERATIONS IN TIME-OUT CONFIGURATION REGISTER; see Fig.11						
$t_{W(WR)}$	$\overline{WR}$ pulse width		10	–	–	ns
$t_{WR(TOC)}$	$\overline{WR}$ LOW to bit CRED = 1	note 1	$\frac{1}{PSC}$	–	$\frac{2}{PSC}$	ETU

Note

1. PSC is the programmed prescaler value (31 or 32).

14 APPLICATION INFORMATION

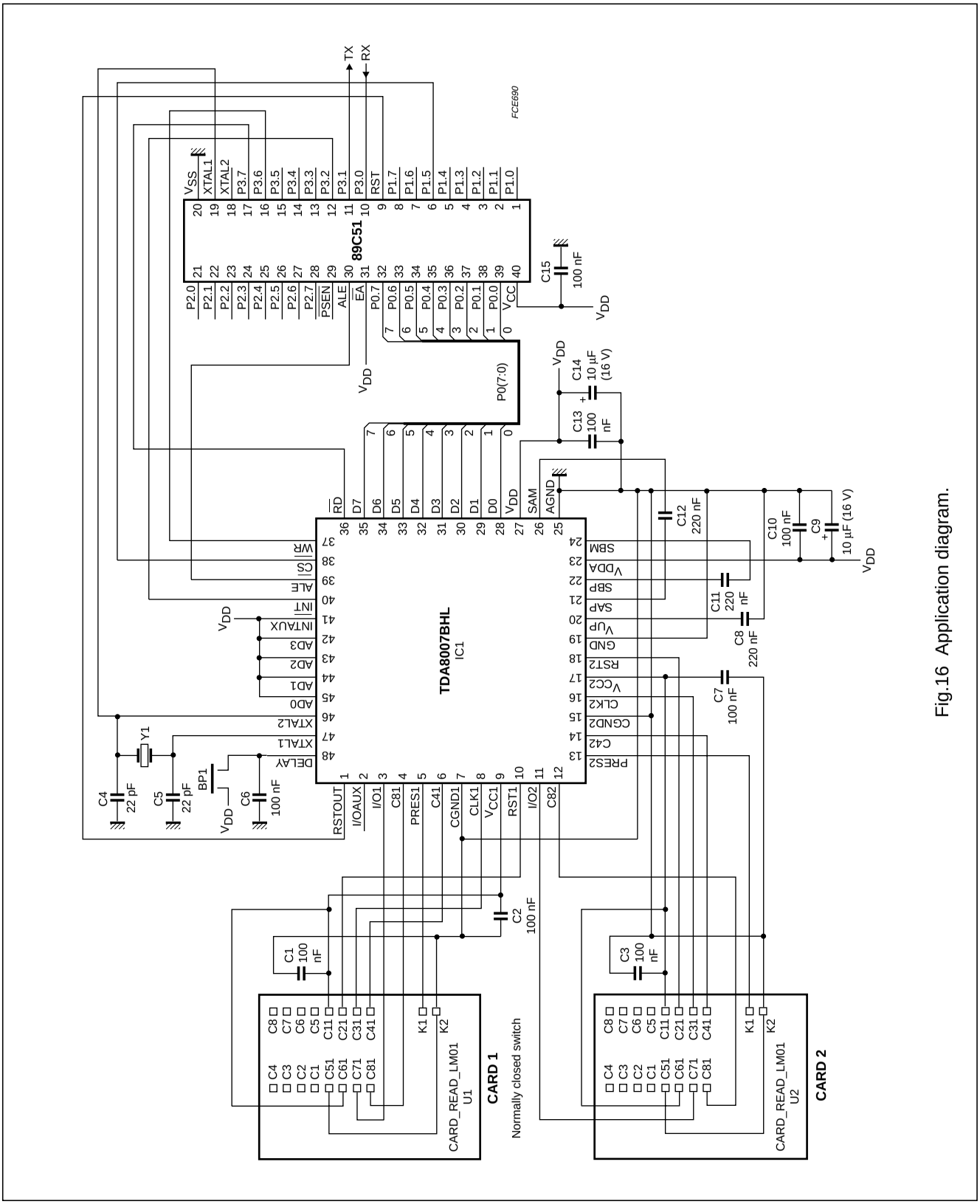
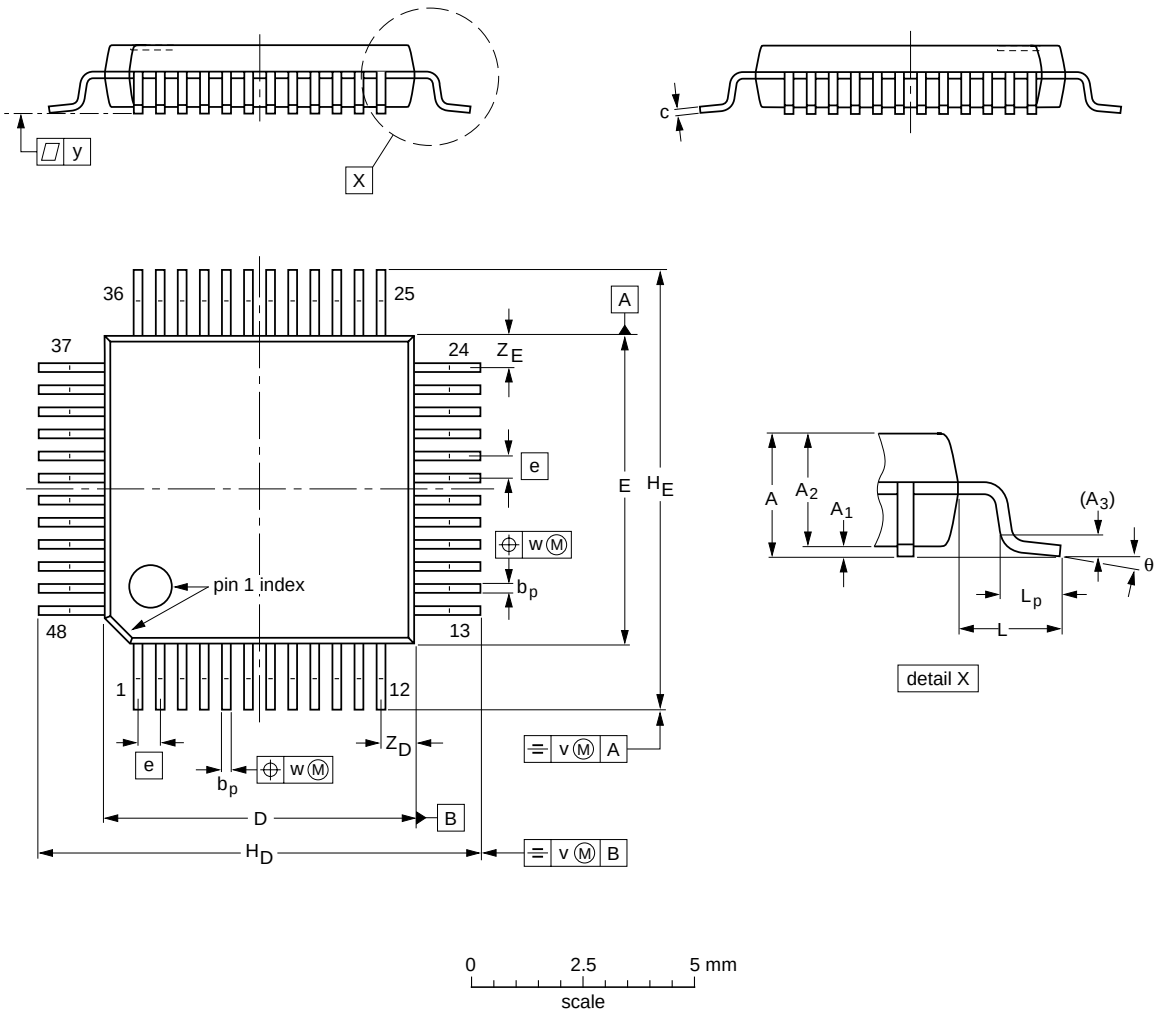


Fig.16 Application diagram.

15 PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2	136E05	MS-026				~~99-12-27~~ 00-01-19

16 SOLDERING

16.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

16.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

16.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

16.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

16.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

17 DATA SHEET STATUS

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Printed in The Netherlands 753504/06/pp48 Date of release: 2003 Feb 18 Document order number: 9397 750 10784

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